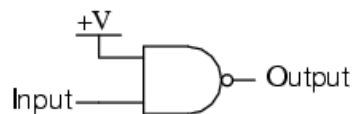


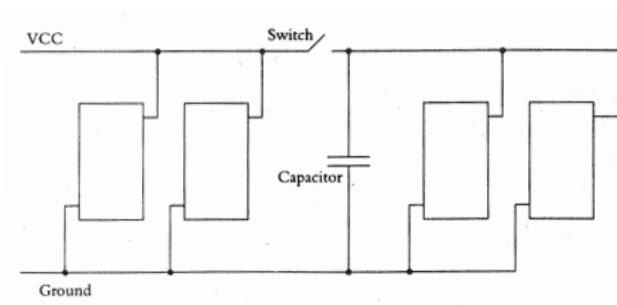
```

graph LR
    In1 --- G1_1[AND Gate 1]
    In1 --- G2_1[AND Gate 2]
    In1 --- G3_1[AND Gate 3]
    In1 --- G4_1[AND Gate 4]
    In0 --- G1_2[AND Gate 1]
    In0 --- G2_2[AND Gate 2]
    In0 --- I1[Inverter 1]
    In0 --- I2[Inverter 2]
    I1 --- G3_2[AND Gate 3]
    I2 --- G4_2[AND Gate 4]
    G1_1 --- Out3
    G2_1 --- Out2
    G3_1 --- Out1
    G4_1 --- Out0
  
```

Input  Output

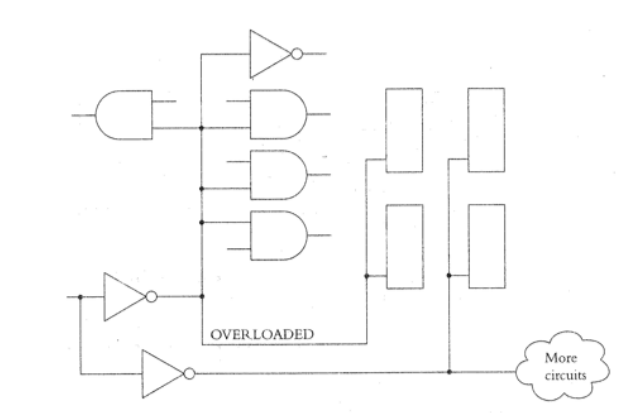


4) Look at the following circuit. The idea is that the circuitry on the left side is always running, but the circuitry on the right side gets turned on and off, using the switch, from time to time in order to save some power.

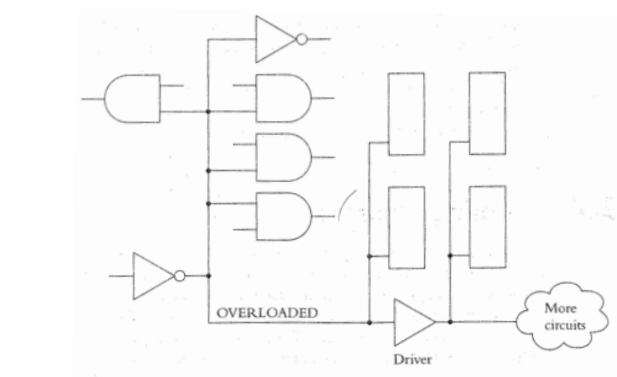


but the circuitry on the right side gets turned on and off, using the switch, from time to time in order to save some power. The capacitor shown in the middle of the diagram is to cushion the voltage when the switch is closed. What is wrong with this design? What are the symptoms most likely be? How should it be fixed?

5.a) How does the following circuit solve the loading problem?



b) How does the circuit on part a) compare to the following circuit?



6) What does the timing diagram look like for a static RAM cell. Remember to include a read and write operation. Hint: Static RAM parts look much like ROM parts, except that they have a write enable signal.