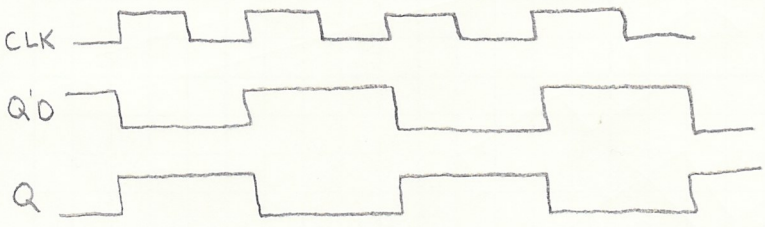
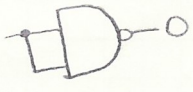
① This is a decoder.

In_1	In_0	$\overline{In_1}$	$\overline{In_0}$	Out3	Out2	Out1	Out0
0	0	1	1	0	0	0	1
0	1	1	0	0	0	1	0
1	0	0	1	0	1	0	0
1	1	0	0	1	0	0	0

② 

CLK	D	$\bar{Q}$	Q
0	0	0	1
0	1	1	0
1	0	0	1
1	1	1	0

The circuit produces a square wave that can only change on the active clock edge. Therefore, it has a 50% duty cycle and only half of the clock's frequency.

③ 

I_1	I_2	O
1	1	0
0	0	1

V	I	O
1	1	0
1	0	1

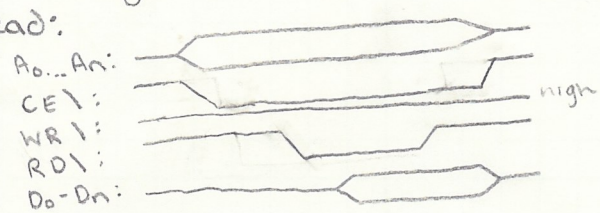
These circuits act as inverters. You would do this to save power. The second circuit is better because it draws less power. The first circuit has two changing inputs, so it draws twice as much power to change its inputs. The second circuit has a set input, so it does not need as much power.

④ This design is wrong because the capacitor is after the switch. This design wont cushion the voltage - it will make it worse. It is located on a straight wire and would therefore draw the current right to ground. If you put the capacitor before the switch it will draw current to the other packages.

⑤ a) This circuit has an extra inverting chip which allows for enough current to go through to the other elements.

b) This circuit has a buffer, which supplies enough current so that the line is not overloaded. There is a higher level of propogation as well: it has three vs. the two levels of the first circuit.

⑥ Read:



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