CPE355 - Real time embedded kernels - Spring'11

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Homework Assignment #3

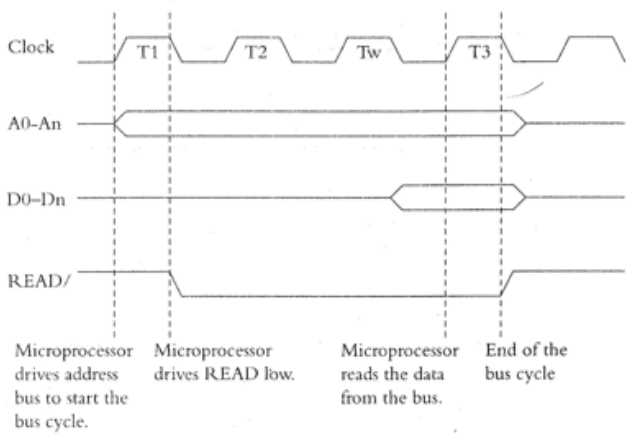
Due date: 11am, Tuesday, January 31st 2012

Homework turned in after the deadline, will not be graded.

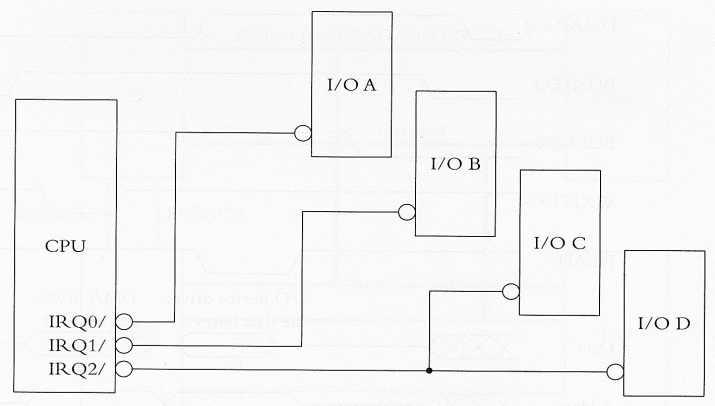
1) (30pts) Suppose that your system has two ROM chips and two DRAM chips whose sizes and addresses are shown in the following table. Design part of the circuit that takes the address lines and produces the chip enable signals for each of these four memory parts.

	Size	Low Address	High Address
ROM	128KB	0x00000	0x1ffff
ROM	128KB	0x20000	0x3ffff
RAM	64KB	0x80000	0x8ffff
RAM	64KB	0x90000	0x9ffff

2) (30pts) Suppose we are using 120 nanosecond ROMS (which have valid data on the bus 120 nanoseconds after the falling edge of OE/) and are using a micro-processor with the following timing diagram, with a clock rate of 25MHz (period is then 40 nanoseconds). How many wait states must the processor insert into each bus cycle that reads from the ROM?



3) (10pts) What are the advantages and disadvantages of hooking up device C and D to the same interrupt pin?



4) (10pts) We did not discuss this in class, but you should be able to find information about this on the internet. Explain what is the difference between a edge-triggered and a level-triggered interrupt? What are the advantages and disadvantages of either implementations?