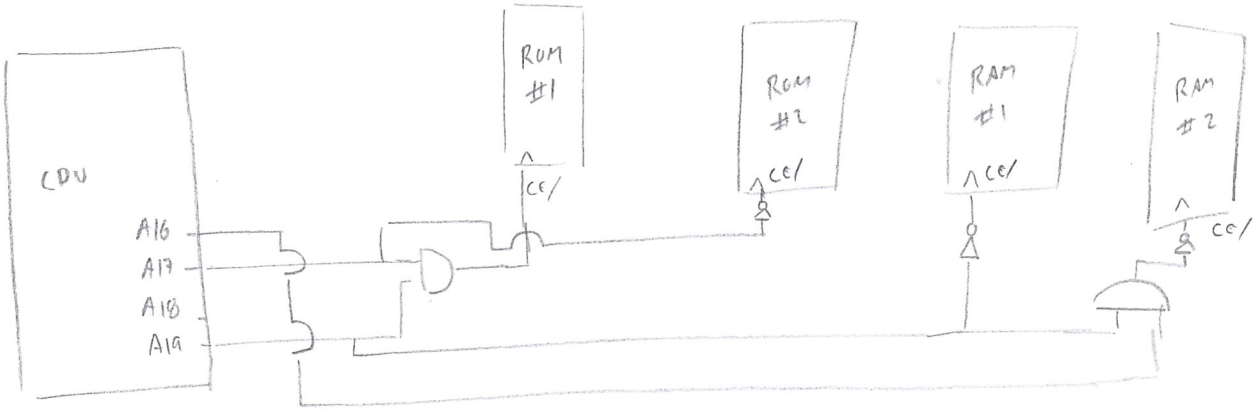
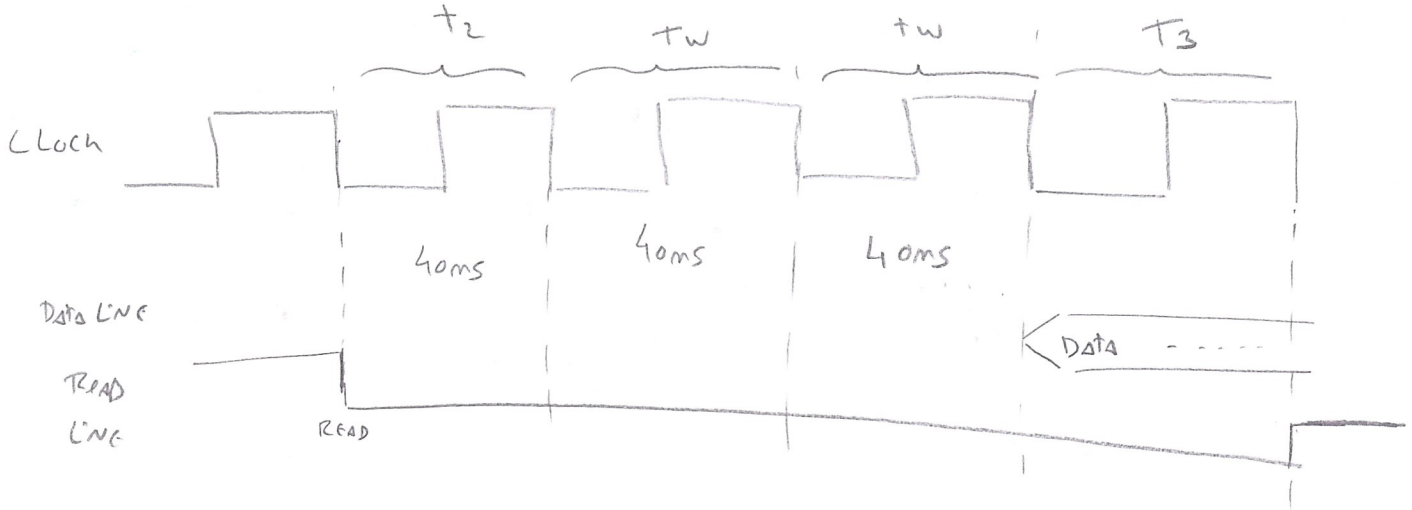
①

	Low Address	High Address
ROM #1	bit 17 & bit 19	Are always 0
ROM #2	bit 17	is ALWAYS 1
RAM #1	bit 19	is ALWAYS 1
RAM #2	bit 16 & bit 19	Are ALWAYS 1



②



③

ADVANTAGES: - Requires less interrupt bus lines

DISADVANTAGES: - it is hard to specify interrupts with different priorities in the same interrupt line.

A **level-triggered interrupt** is an interrupt for which an unserviced interrupt is indicated by a particular state, high level (or low level), of the interrupt request line. The interrupt request line will remain either high (or low) until the interrupt has been handled.

These type of interrupts are useful for systems that may have lots of voltage fluctuations (noise) in the interrupt line. Level-triggered interrupts are also useful if multiple I/O devices are sharing the same interrupt lines, since the CPU no longer has to check multiple I/Os for interrupts. Unfortunately having multiple I/O sharing the same line will yield to the inability to distinguish between higher priority and lower priority I/O devices. Sharing interrupt lines also poses a problem if the CPU cannot possibly resolve a particular interrupt; all I/O devices on that particular interrupt line will be blocked.

A **Edge-triggered** interrupt is signaled by a level transition on the interrupt line, either a falling edge (high to low) or a rising edge (low to high). A device wishing to signal an interrupt drives a pulse onto the line and then releases the line to its inactive state. A big disadvantage of this implementation is that we need to ensure that the pulse is adequately long so it can be detected without any special hardware. Fortunately these type of interrupts do not suffer the problems that level-triggered interrupts have with sharing. Service of a low-priority device can be postponed arbitrarily, and interrupts will continue to be received from the high-priority devices that are being serviced.