Western New England College
College of Engineering

CPE 462 - VHDL: Simulation and Synthesis - Fall 2011

MWF 10:00 am to 10:50 am @ Sleith-101

http://www.nunoalves.com/classes/fall11-cpe462

Instructor: Prof. Nuno Alves

Contact Information: 401-633-4660 or nalves@wne.edu

Office Hours: MW 11:00am to 11:50am at S-313

Pre-requisite: Digital Design (CPE 271) and knowledge of any programming language.

Course Description: This is an introductory course in reconfigurable computing with the VHDL language. This is an extremely hands on course in which students will learn enough about the language to describe most digital hardware, including processors, interface circuits, etc. Students will learn how to use a simulator program to verify the correctness of their description. Finally students will synthesize programmable devices using VHDL. Several simulation exercises and synthesis projects are included.

Required Material: No required textbook.

Supplementary Materials: The recommended textbooks are,

- "RTL hardware design using VHDL" by Chu, 2006 Wiley-Interscience
- "Circuit design with VHDL" by Volnei A. Pedroni, 2004 MIT Press.

Learning Objectives and Assessment: After taking the course, students should be able to:

Objectives/Outcomes	Assessment Techniques
Write VHDL descriptions of digital hardware and test-benches for those descriptions.	Assignments, exams
Use VHDL features such as functions, procedures, components, and generics to describe hardware.	Assignments, exams
Use synthesis software to implement VHDL descriptions. Perform post-implementation simulation to verify circuit is correct. Program and test programmable chip.	Assignments

Course Requirements:

1. *Assignments* (70% of final grade)*:* There will be regular take-home graded assignments These will cover the most important class related topics and will usually consist of practical implementations. A possible solution will be posted on the course website after its due date.

2. *Examinations* (30% of final grade): There will be two hour-long exams throughout the course. These exams will consist of VHDL simulation exercises at a computer.

Grading: The range of numerical grades and the traditional letter equivalents are as follows:

A 93-99	B+ 87-89	C+ 77-79	D+ 67-69	F 55-59
A- 90-92	B 83-86	C 73-76	D 60-66	
	B- 80-82	C- 70-72		

Exam Policy: In case of convincing emergencies or medical conditions you may retake the exam at a later date.

Attendance Policy: While it is college policy is that students are expected to attend all class sessions for courses in which they are enrolled, students will not be penalized if they do not show up to regular classes.

Mid-Semester Grades: Instructors are required to submit mid-semester grades. These mid-term grade will reflect the instructor's actual evaluation of student's progress.

Integrity of Scholarship from the College catalog: "Honesty in all academic work is expected of every student. This means giving one's own answers in all class work, quizzes, and examination without help from any sources not approved by the instructor. Written material is to be the student's original composition. Appropriate credit must be given for outside sources from which ideas, language, or quotations are derived".

Other Information:

1. Student grades will be posted regularly on manhattan (https://manhattan.wnec.edu). Manhattan will **not** be used for anything else.

2. Classes will be a mixture of hands on laboratory work and standard presentation of material and examples. Class discussion and participation is encouraged. Generally, an assignment will be given at the end of each class-topic which will be due at a specified date. On some dates, the class will meet at another location, Sleith-209.

3. There are several open research problems that are related to the topics discussed in this class. Please contact me during office hours if you are interested in partaking in some research projects. The outcome of these research projects will not impact your grade in this class. Also, keep in mind, that any research collaboration will require a considerable time commitment.

4. Changes in syllabus and assignment sheet may be modified as deemed appropriate. All changes will be announced in class.

5. Students with a disability who are requesting academic accommodations should contact the SDS office in Deliso GO6, or call 782-1257/1528 for an appointment.

6. Any student who is unable, because of his religious beliefs, to attend classes or to participate in any examination, study, or work requirement on a particular day shall be excused from any such examination or study or work requirement, and shall be provided with an opportunity to make up such examination, study, or work requirement which he may have missed because of such absence on any particular day; provided, however, that such makeup examination or work shall not create an unreasonable burden upon such school.

7. For each assignment, you must complete and turn in your work by the assigned date, in order to be graded in full credit. Any work turned in within 24 hours after the due date will be penalized by 10% of the full credit; any work turned in within the time between 24 hours and 48 hours of the due date will be penalized by 30% of the full credit; any work turned in within the time between 48 hours and 72 hours of the due date will be penalized by 50% of the full credit. No work will be accepted after the third day after the

due date. Of course, there will be exceptions for convincing emergencies and medical conditions.

8. Faculty evaluations will be administered at the end of the semester.

Material covered:

1. Introduction to reconfigurable computing architectures

2. Review of digital signals

3. Use of software

4. Use of Spartan FPGA boards

5. Introduction, structure of VHDL descriptions

6. Signals, signal assignment statements

7. Test-benches

8. Processes

9. Sequential Circuit descriptions

10. Components

11. State Machines

12. Generic parameters

13. Synthesis Issues in sequential circuits

14. Functions, procedures, packages

15. User defined data types

16. Use of on-chip memory