CPE462 - VHDL: Simulation and Synthesis - Fall'11

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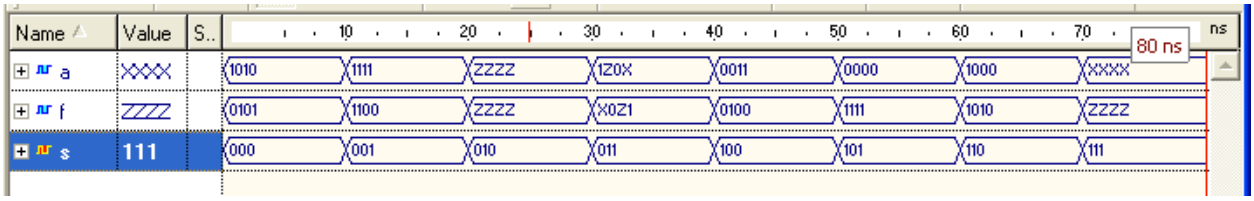
Midterm Exam #1 Solutions

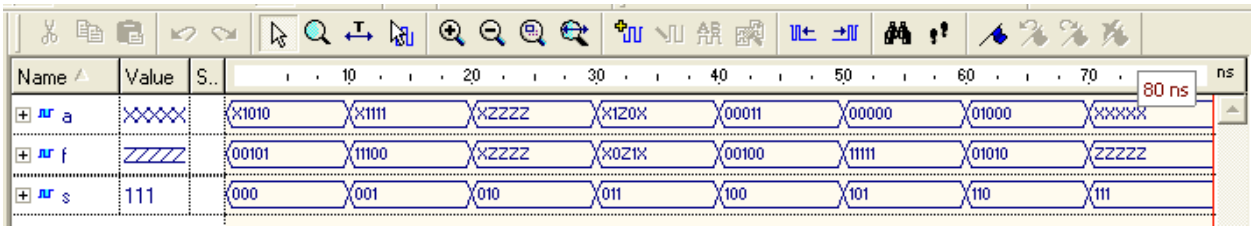
Wave-form for question #1



Code for question #1:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity question1 is
        port (a : in std_logic_vector(3 downto 0);
        s : in std_logic_vector (2 downto 0);
        f : out std_logic_vector (3 downto 0)
        );
end entity;

architecture myarch of question1 is
        signal ouputShift : std_logic_vector(3 downto 0);
        signal outputInc  : std_logic_vector(3 downto 0);

        signal a_bitvector : bit_vector (3 downto 0);
        signal a_reverse : std_logic_vector (3 downto 0);


begin
        --temporary signal assigments
        a_bitvector <=  to_bitvector(a);

        loop1: for i in a'range generate
                a_reverse(a'high - i) <= a(i);
        end generate;


        --shift block
        with s(1 downto 0) select
        ouputShift <= to_stdlogicvector(a_bitvector srl 1) when "00",
                        to_stdlogicvector(a_bitvector sll 2) when "01",
                        a when "10",
                        a_reverse when others;

        --incrementer block
        with s(1 downto 0) select
        outputInc <= a+1 when "00",
                        a-1 when "01",
                        a+2 when "10",
                        (Others=>'Z') when others;

        --2-to-1 mux block
        with s(2) select
        f <= outputInc when '1',
                        ouputShift when others;

end architecture;
```

Wave-form for question #2



Code for question #2:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity question1 is
        generic (n: integer := 5);
        port (a : in std_logic_vector(n-1 downto 0);
        s : in std_logic_vector (2 downto 0);
        f : out std_logic_vector (n-1 downto 0)
        );
end entity;

architecture myarch of question1 is
        signal ouputShift : std_logic_vector(n-1 downto 0);
        signal outputInc  : std_logic_vector(n-1 downto 0);

        signal a_bitvector : bit_vector (n-1 downto 0);
        signal a_reverse : std_logic_vector (n-1 downto 0);


begin
        --temporary signal assigments
        a_bitvector <=  to_bitvector(a);

        loop1: for i in a'range generate
                a_reverse(a'high - i) <= a(i);
        end generate;


        --shift block
        with s(1 downto 0) select
        ouputShift <= to_stdlogicvector(a_bitvector srl 1) when "00",
                        to_stdlogicvector(a_bitvector sll 2) when "01",
                        a when "10",
                        a_reverse when others;

        --incrementer block
        with s(1 downto 0) select
        outputInc <= a+1 when "00",
                        a-1 when "01",
                        a+2 when "10",
                        (Others=>'Z') when others;

        --2-to-1 mux block
        with s(2) select
        f <= outputInc when '1',
                        ouputShift when others;

end architecture;
```

Test-bench for question #2:

```
library ieee;
use ieee.std_logic_1164.all;

entity test_question1 is
end;

architecture bench of test_question1 is
constant n: positive:=5;
component question1
        generic (n: integer := n);
        port (a : in  std_logic_vector(n-1 downto 0);
                  s : in  std_logic_vector (2 downto 0);
                  f : out std_logic_vector (n-1 downto 0)
        );
  end component;

  signal a : std_logic_vector (n-1 downto 0);
  signal s : std_logic_vector (2 downto 0);
  signal f : std_logic_vector (n-1 downto 0);

begin
 a   <= "X1010",
 "X1111" after 10ns,
 "XZZZZ" after 20ns,
 "X1Z0X" after 30ns,

 "00011" after 40ns,
 "00000" after 50ns,
 "01000" after 60ns,
 "XXXXX" after 70ns;


 s   <=
 "000",                -- f=a shift right
 "001" after 10ns,     -- f=a shift left 2 units
 "010" after 20ns,     -- f=a unchanged
 "011" after 30ns,     -- f=a reverse bits
 "100" after 40ns,     -- f=a+1
 "101" after 50ns,     -- f=a-1
 "110" after 60ns,     -- f=a+2
 "111" after 70ns;     -- f=ZZZZZ
 m: question1 port map (a,s,f);

end bench;
```