CPE462 - VHDL: Simulation and Synthesis - Fall'II

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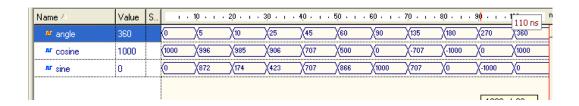
Exam instructions:

- I. You have learned many different VHDL constructs. You may use any construct you want, as long as your program is synthesizable in hardware.
- 2. You grade will not be based on code aesthetics, but on performance.
- 3. The exam will be made available Monday, Dec. 12 at 11:00am and it is due Wednesday, Dec. 14 at 11:00am.
- 4. Late exams will receive a grade of zero. There is absolutely no grace period! So submit early to avoid any problems.
- 5. You are NOT allowed to communicate with anyone else regarding this exam.
- 6. You are also NOT allowed to copy code from other sources except class slides.
- 7. Once you are done with the exam, email nalves@wne.edu a copy of your exam in a word document. Use the font **Courier New** for your report.

The exams will be graded by 3pm on Wednesday afternoon. Pick them before 6pm of Friday, Dec. 16.

Question I: Geometric Procedure

Create a VHDL program with a procedure in the same file (no packages are necessary here) that will return the cosine and sine of a particular angle. The input of your program must be an INTEGER representing the angle is degrees (0 to 360). The output must also be an INTEGER representing the function outcome. Because sines and cosines are limited at I and -I, multiply each function by 1000 so you can store the outcome in an integer. Look at the simulation results below for some expected outcomes.



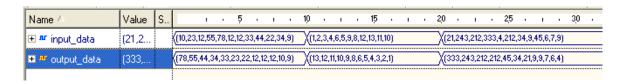
Some comments:

- There are other non-synthesizable data-types we briefly talked in class such as REAL. Do not use them. Your code should only use INTEGERS and should also work on our FPGA boards.
- You program must work with the test-bench available at:

http://www.nunoalves.com/classes/fall11-cpe462/hw/final_exam_q1.txt

Question 2: Sorting Function

Create a function inside a package that will sort the contents of a bus of 12 INTEGER elements. Look at the simulation results below for some expected outcomes.



Some comments:

- A n² time complexity for your sorting algorithm is fine.
- You program must work with the test-bench available at:

http://www.nunoalves.com/classes/fall11-cpe462/hw/final_exam_q2.txt

Question 3: Traffic lights

The controller to be designed controls the traffic lights of a busy highway (HWY) intersecting a side road (SRD) that has relatively lighter traffic load. Figure I shows the location of the traffic lights. Sensors at the intersection detect the presence of cars on the highway and side road. The figures implies that both the highway and side roads offer single lanes for traffic in each direction.

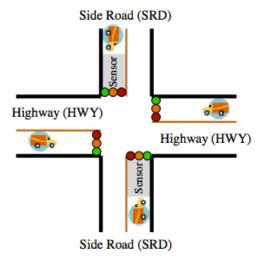


Figure 1: Highway and a side road intersection

In this exercise you will create finite-state machine circuit which will control the traffic lights.

Finite-state machine specifications

The traffic light controller works in the following way.

- I. The lights controller makes use of car sensors at the intersection of the side road with the highway, to sense presence of cars.
- 2. The lights controller makes use of three timers: a 60 seconds timer, a 30 seconds timer, and a 10 seconds timer. You may assume you have a reliable 1Hz clock feeding your traffic light controller.
- 3.Pedestrians can use the intersection by pressing buttons. Pedestrians will need to cross the highway only since crossing the side road is assured most of the time.
- 4. HWY lights remain green as long as there are no cars triggering the SRD sensors or when there are no pedestrians pressing the crossing buttons.

- 5. When HWY lights have been green for a minimum of 60 seconds, a car on SRD, or a pedestrian wanting to cross, will cause HWY lights to cycle through yellow to red states.
- 6. Once the SRD lights become green, they will remain green for 30 seconds.
- 7. Afterwards, SRD lights will cycle through yellow and red states and HWY lights will then turn green.
- 8. The lights always stay yellow for 10 seconds.
- 9. Each traffic post has three lights GREEN, YELLOW and RED.
- 10. In the default state, HWY lights show GREEN and SRD lights show RED.

Design, model and simulate the finite-state machine for the traffic light controller. Using the following entity:

As you can see the two output signals are an enumerated data-type and they contain the traffic light colors (red, green and yellow). In order for this circuit to work you need to have an external package that defines these enumerated data-types.

Your program must work with the test-bench available at:

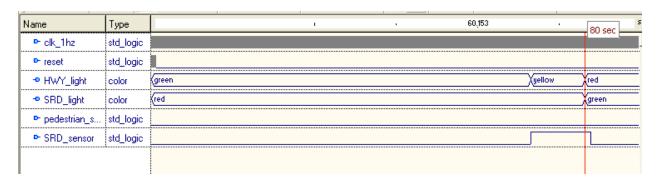
http://www.nunoalves.com/classes/fall I I -cpe462/hw/final_exam_q3.txt

Suggestions:

- Draw the traffic-light controller indicating all I/O control signals.
- Draw a block diagram for the traffic light controller indicating clearly the main system blocks and interface signals.
- Draw a Mealy-style state diagram which covers all legal state transitions of the machine.

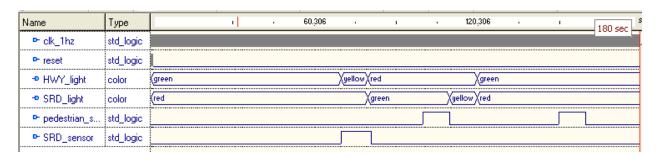
To help you out, here are some expected outputs:

Event #1 (0 seconds to 90seconds): At t=70s, a truck shows up in the service road, and the highway light (which was green for more than 60 seconds) becomes yellow (for 10 seconds) and then red. The truck takes one second to cross the intersection.



Event #2 (0 seconds to 180 seconds): Some gentlemen decides to cross the highway at t=100s and presses the button. But the highway light is red, which means pedestrians can cross without a problem... Idiot!

At t=150s another gentlemen decides to cross the HWY. This time HWY light is green, but it hasn't been green for more than 60 seconds so the light remains green. The pedestrian gets tired of waiting and probably makes a run for it.



Event #3 (0 seconds to 270 seconds): At t=170s, a mini-van shows up in the service road. After 10 seconds, the highway light becomes green for 60 seconds and it will cycle to yellow and then red. However, the mini-van does not move. Seriously? It probably broke down. Oh well, the traffic light does not really care. After 30 seconds, the service road light will turn to yellow and then red. The mini-van doesn't move at all.

