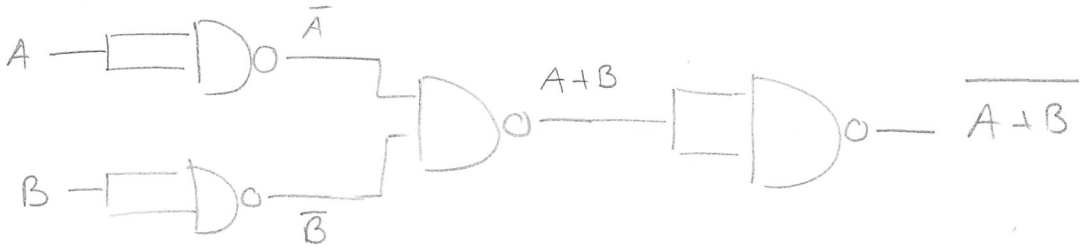
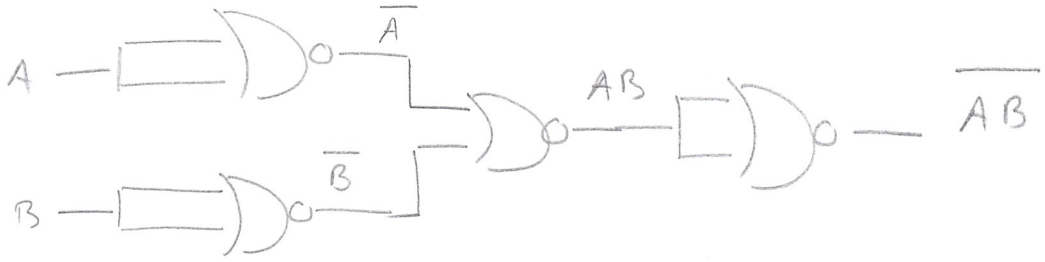
VHDL HW#1

(1) a) NOR GATE WITH NAND GATES

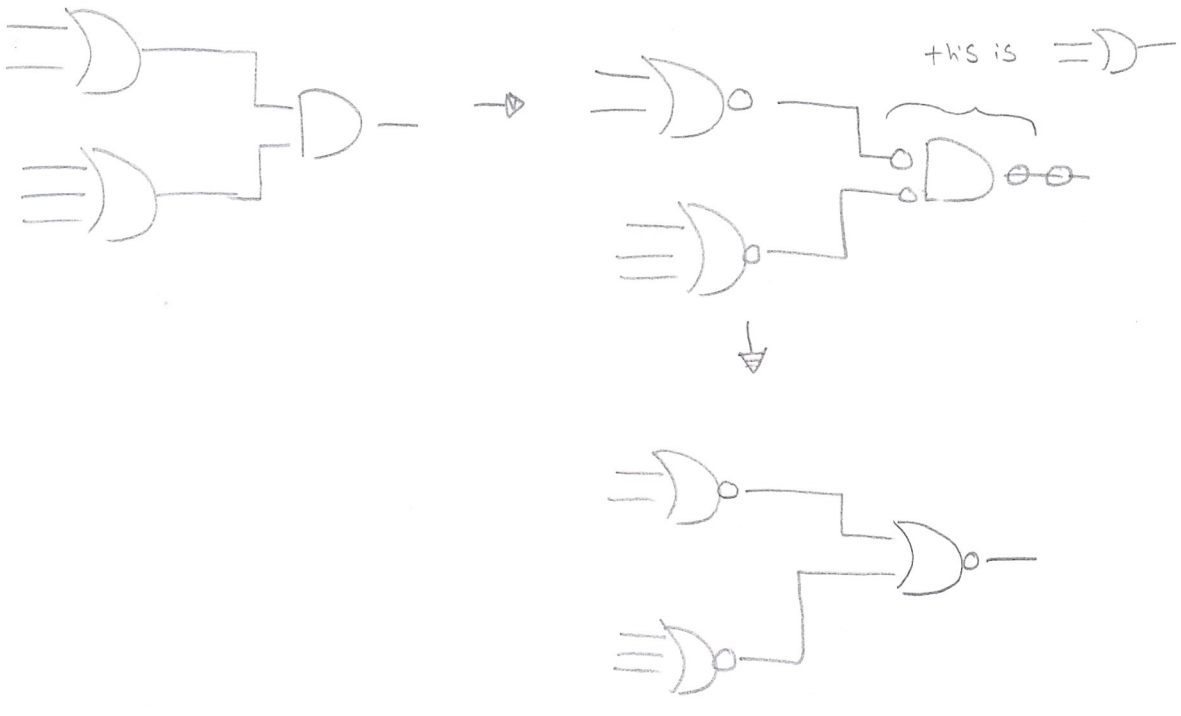
5pts



5pts b) NAND GATE WITH NOR GATES



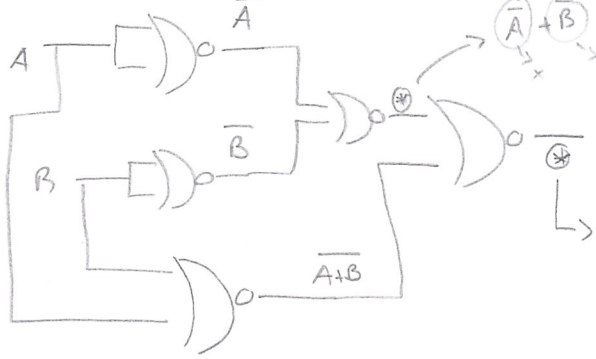
10pts c)



5pts D) it is easier to estimate circuit timmings & Power Consumption.

(2)

10 pts a)



$\overline{(\bar{A}+\bar{B})} = \overline{x+y} = \bar{x}\cdot\bar{y} = \bar{\bar{A}}\cdot\bar{\bar{B}} = AB$

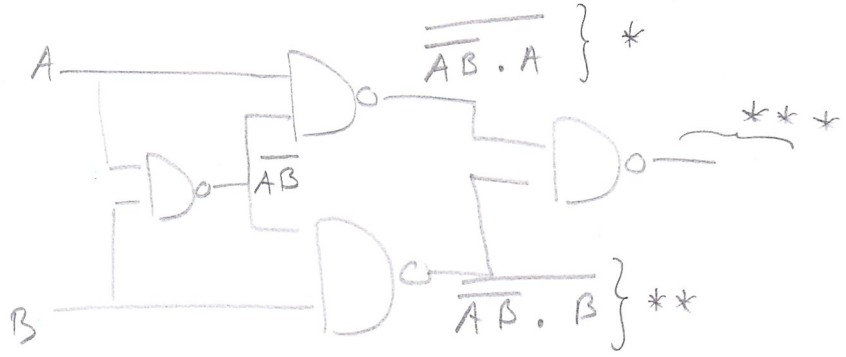
$\overline{(AB)+(\overline{A+B})}$ Let $\overline{A+B} = z$

$\overline{AB+z} = \overline{AB}\cdot\bar{z} =$

$(\bar{A}+\bar{B})\cdot\overline{(\overline{A+B})} = (\bar{A}+\bar{B})\cdot(A+B) =$

$\underbrace{\bar{A}A}_{\emptyset} + \bar{A}B + A\bar{B} + \underbrace{\bar{B}B}_{\emptyset} = \bar{A}B + A\bar{B}$

10pts b)



(*) Let $\overline{AB} = X$ => $\overline{\overline{AB}\cdot A} = \overline{X\cdot A} = \overline{X}+\bar{A} = \overline{\overline{AB}}+\bar{A} = AB+\bar{A}$

(**) Let $\overline{AB} = Y$ => $\overline{\overline{AB}\cdot B} = \overline{Y\cdot B} = AB+\bar{B}$

(***) $\overline{(AB+\bar{B})\cdot(AB+\bar{A})} = \overline{(AB+z)\cdot(AB+w)} = \overline{(AB+z)}+\overline{(AB+w)}$

Let $\bar{B} = z$, $\bar{A} = w$

$= \left[\overline{(\overline{AB}\cdot\bar{z})}\right] + \left[\overline{(\overline{AB}\cdot\bar{w})}\right] = \left[\overline{(\bar{A}+\bar{B})}\cdot B\right] + \left[\overline{(\bar{A}+\bar{B})}\cdot A\right]$

$= \bar{A}B + \bar{B}B + A\bar{B} + A\bar{A} = \bar{A}B + A\bar{B}$

(3) $a + [(\overline{b.c}).a] = d$

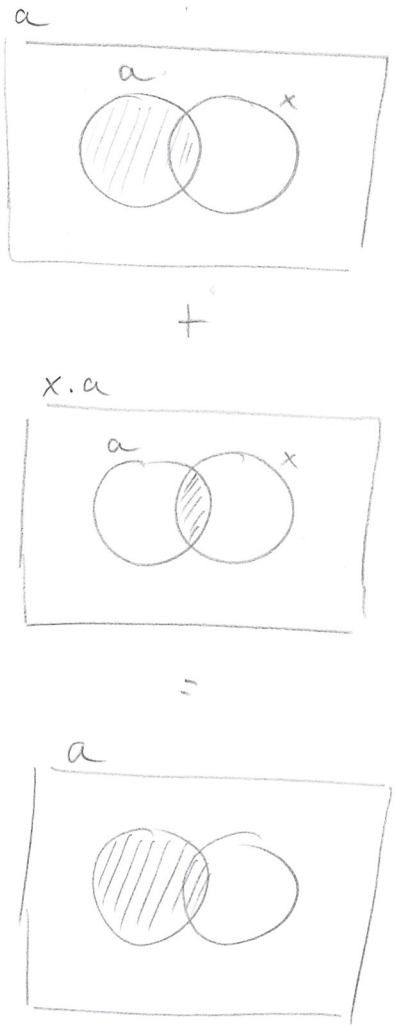
10pts

let $\overline{b.c} = x$

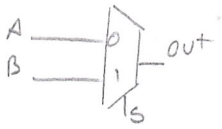
$a + [x.a] = d$

by the absorption law ⟶

$a = d$



(4)



$OUT = A\bar{S} + BS$

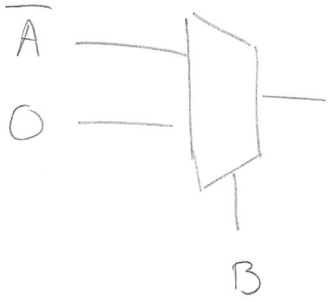
10pts a) NOT GATE:

$OUT_a = 1\bar{A} + 0A$

5) NOR GATE WITH A MUX

Remember $\overline{A+B} = \overline{A} \cdot \overline{B}$

10pts

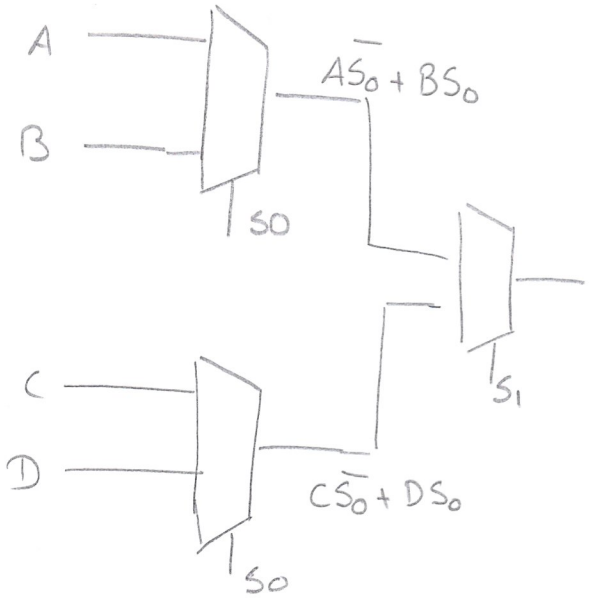


$OUT_5 = \overline{A}\,\overline{B} + 0B = \overline{A}\,\overline{B}$

$= \overline{A+B}$

(5)

10pts

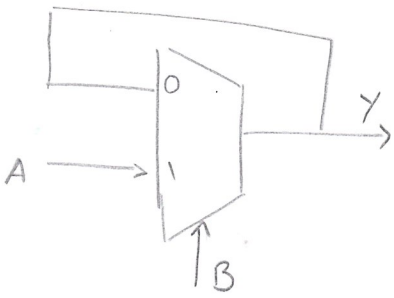


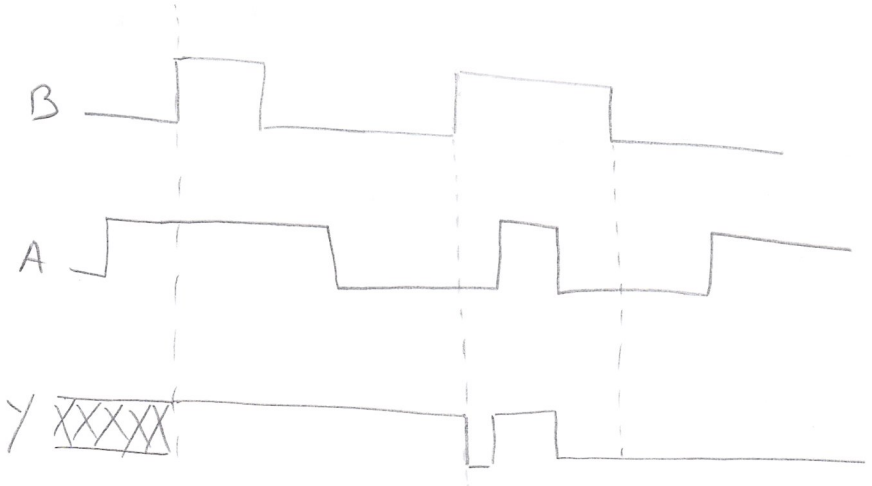
$OUT = (A\overline{S_0} + BS_0)\,\overline{S_1} + (C\overline{S_0} + DS_0)\,S_1$

$= A\overline{S_0}\,\overline{S_1} + BS_0\,\overline{S_1} + C\overline{S_0}\,S_1 + DS_0S_1$

(6)

5pts





This is A LATCH

(7) 5pts

a) 3 clock cycles

b) 1 clock cycle

c) 3 clock cycles

(8) 5pts

- IN A FLIP FLOP, THE INPUT IS ONLY PROPAGATED TO AN OUTPUT AT A CLOCK EDGE (EITHER RISING, FALLING or both)
- IN A LATCH, THE INPUT PROPAGATES TO THE OUTPUT WHENEVER CLOCK IS HIGH