CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #1

Due: Friday, September 9th 2011 @ the beginning of our class.

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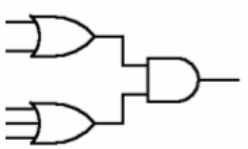
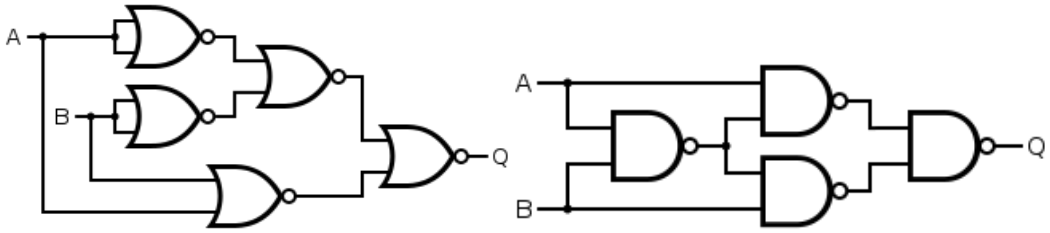
1. We discussed universal gates.
   a. With only NAND gates, come up with a circuit schematic for a NOR gate.
   b. With only NOR gates, come up with a circuit schematic for a AND gate.
   c. Create an equivalent representation of the following circuit using just NOR gates.



   d. In a couple of lines describe why do you think we should care about describing a circuit with just a single type of universal gates.

2. Using either boolean logic, or graphical representations of De'Morgan rules, show that the following two circuits are indeed equivalent to an XOR gate (AB' + BA').



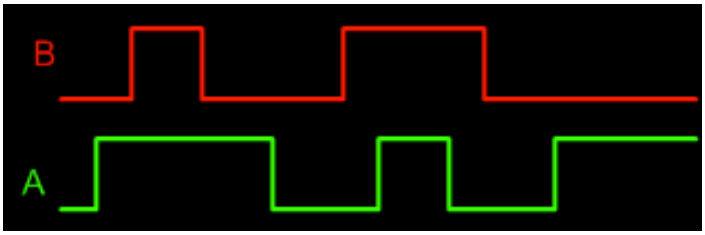
3. Simplify the following expression and draw its equivalent circuit:

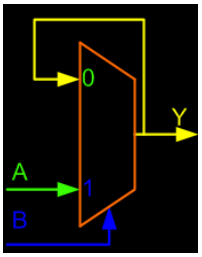
$$a + \left((\overline{b \cdot c}) \cdot a \right) = d$$

4. With any number of 2-to-1 MUX gates, implement the following gates:
   a. NOT
   b. NOR

5. Build a 4-to-1 MUX using just 2-to-1 MUX gates.

6. Look at the following circuit and its sample input waveform. Draw the Y-waveform .What is the circuit equivalent to?



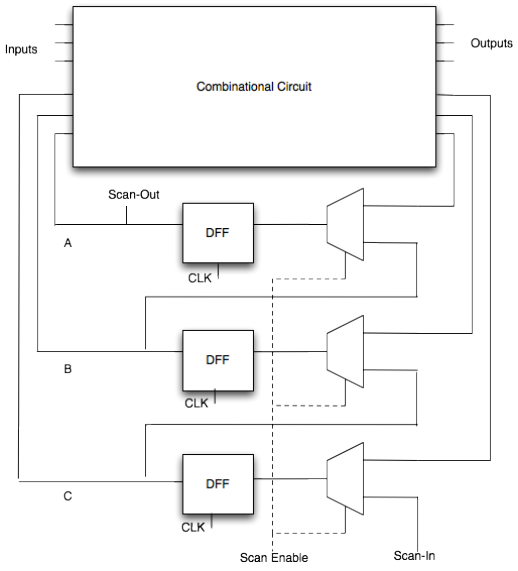


7. In the following scan-chain architecture, how many clock cycles will it take to:

a) set A=0, B=0 and C=1

b) simulate the combinational circuit with these new inputs

c) read new values of A, B and C



8. What is the difference between a latch and a flip-flop?