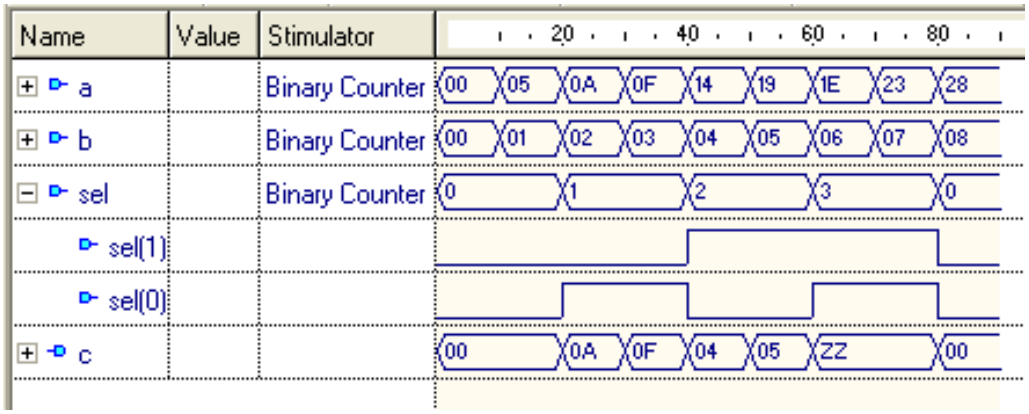
WESTERN NEW ENGLAND UNIVERSITY | WNE

1.

main program

```
library ieee;
use ieee.std_logic_1164.all;
entity mux is
  port (a, b:in std_logic_vector(7 downto 0);
        sel: in std_logic_vector(1 downto 0);
        c: out std_logic_vector(7 downto 0));
end mux;
architecture example of mux is
begin
  process (a, b, sel)
  begin
      if (sel="00") then
           c <= "00000000";
      elsif (sel="01") then
           c <= a;
      elsif (sel="10") then
           c <= b;
      else
           c <= "ZZZZZZZZ";
      end if;
  end process;
end architecture;
```



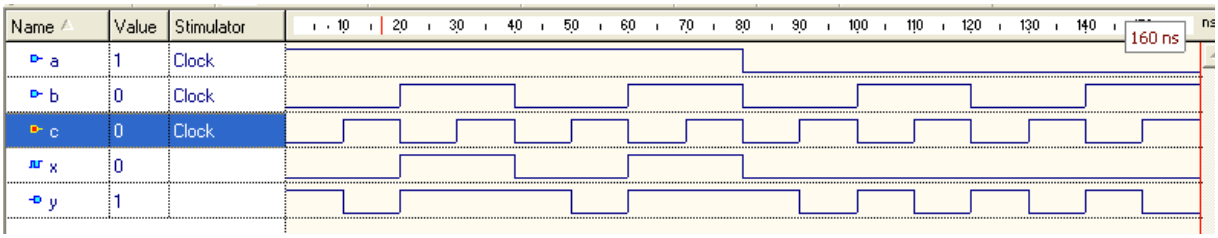
2.

main program

```
entity circuit is
      port(a, b, c: in bit;
      y: out bit);
end circuit;

architecture myarch of circuit is
      signal x : bit;
begin
      x <= a and b;
      y <= x OR (not c);
end architecture;
```

The signal A,B and C will have the respective frequencies of 12.5 MHz, 25MHz and 50 MHz. So the period for each signal is 80ns, 40ns and 20ns.



Bellow is the truth table from the assignment. Both the truth table and the waveforms match.

a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Grading criteria:

Q1 (50 points):

- Missing or incorrect code: -30
- Waveforms (pick one)
    - Missing or incorrect waveform: -20
    - Incomplete / unclear waveform: -5

Q2 (50 points):

- Code (pick one)
    - Missing or incorrect code: -30
    - Inefficient implementation (e.g. use of inout ports): -5
- Waveforms (pick one)
    - Missing or incorrect waveform: -20
    - Incomplete / unclear / done with other methods besides clocks: -10