CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #2

Due Date: Friday, September 16th 2011

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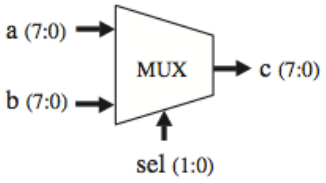
1. Look at the following MUX and its respective truth table. For example, if **sel**='10' then the output is whatever 8 bits that were provided in input **a**. If **sel**='11' then we want the output to be in a high impedance state(Z). Setting up a signal to an high impedance state is obtained with the VHDL command output <= "Z". If you have 8 bits, then you should add the command output <= "ZZZZZZZZ" .



sel	c
00	0
01	a
10	b
11	Z

a) Look at the code below and fill in the blanks

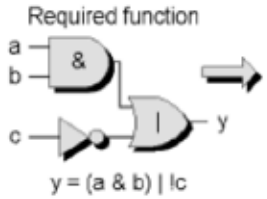
b) With active HDL or Xilinx ISE, check the syntax and provide some input/output waveforms. Turn in a printout of the code and a screenshot of the waveforms.

```
library ieee;
use _____________________________;

entity mux is
    port (___, ___: ___ std_logic_vector(7 downto 0);
          sel: in ____________________;
          ___: out std_logic_vector(7 downto 0));
end mux;

architecture example of _____ is
begin
    process (a, b, sel)
    begin
       if (sel="00") then
           c <= "00000000";
       elsif (__________) then
           c <= a;
       elsif (sel="10") then
           c <= _____;
       else
           c <= "_________";
       end if;
    end __________;
end __________;
```

2. a) Implement the following function in VHDL using active HDL. Printout the source-code.



a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

b) Generate the waveforms for all 8 input combinations using 3 different clocks. Write down the frequency for each clock and take a screenshot of the input/output waveforms. Make sure you press the option zoom-to-fit, so that the entire wave covers a single screen.