CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #3

Due Date: Monday, September 26th 2011

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1. Look at the following signal declarations:

```
TYPE array1 IS ARRAY (7 DOWNTO 0) OF STD_LOGIC;
TYPE array2 IS ARRAY (3 DOWNTO 0, 7 DOWNTO 0) OF STD_LOGIC;
TYPE array3 IS ARRAY (3 DOWNTO 0) OF array1;

SIGNAL a : BIT;
SIGNAL b : STD_LOGIC;:
SIGNAL x : array1;
SIGNAL y : array2;
SIGNAL w : array3;
SIGNAL z : STD_LOGIC_VECTOR (7 DOWNTO 0);
```

   a. What is the dimensionality for each of the signals (scalar, 1D, 2D, or 1Dx1D)?
   b. Write down an assignment example for each signal.
   c. Which of the following assignments are legal or illegal? Write a short explanation for each. Determine the dimensionality on both sides of the assignment.

Assignment	Dimension (on each side)	Legal or illegal (why)
`a <= x(2);`		
`b <= x(2);`		
`b <= y(3,5);`		
`b <= w(5)(3);`		
`y(1)(0) <= z(7);`		
`x(0) <= y(0,0);`		
`x <= "1110000";`		
`a <= "0000000";`		
`y(1) <= x;`		
`w(0) <= y;`		

2. A ROM (read-only memory) can be done with a 1Dx1D array that is CONSTANT. This particular ROM block that you are going to design needs to have eight cells of four bits each.
   a. Create an array called rom, then define a signal of type rom capable of solving this problem. Pick 8 different non-zero value for each of the ROM addresses and this array as a CONSTANT (instead of a SIGNAL) , that is, "CONSTANT my_rom: rom :=(values);". Turn in a printout of your code.

b. Create a test-bench that will simulate the extraction of all 8 ROM values. Turn in a printout of your test-bench and the resulting waveform.

3. Look at the following solution for a 4-bit adder.

main code with signed data types

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity adder1 is
     port (a, b : in signed (3 downto 0);
            sum : out signed (3 downto 0));
end entity;

architecture adder1 of adder1 is
begin

     sum <= a + b;

end architecture;
```

All signals are of type SIGNED. Notice also the inclusion of the std_logic_arith package (line 4), which specifies the SIGNED data type. Recall that a SIGNED value is represented like a vector; that is, similar to STD_LOGIC_VECTOR, not like an INTEGER.

a. Rewrite this solution with all input and output signals of type STD_LOGIC_VECTOR. Turn in a printout of your code.

b. Download the test-bench from the class website, simulate the circuit and turn in a printout of the resulting waveform. This test-bench is available at :

http://www.nunoalves.com/classes/fall11-cpe462/hw/hw03_ex3-testbench.vhd