CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #4

Due Date: Friday, September 30th 2011

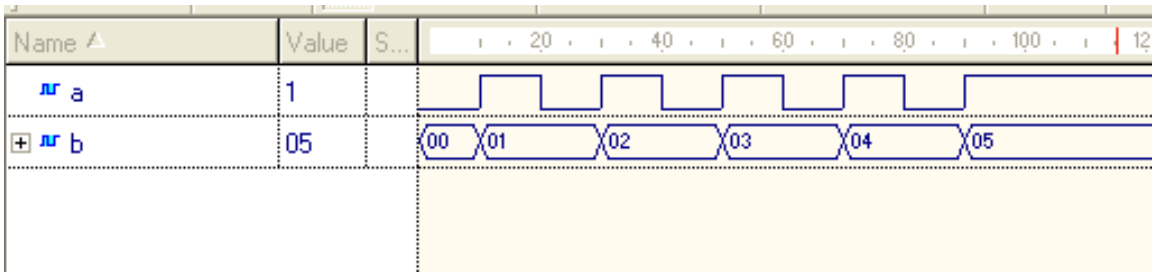
1.

main code (part a)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity incrementer is
      port (a : in std_logic;
      b : out std_logic_Vector (7 downto 0)
      );
end entity;

architecture myarch of incrementer is
      signal x : std_logic_vector(7 downto 0) := "00000000";
begin
      process(a)
      begin
            if (a='1') then x <= x + 1;
            end if;

      end   process;

       b <= x;
end architecture;
```

test-bench code (part b)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity testmain is
end;

architecture bench of testmain is
  component incrementer
     port (a : in std_logic;
           b : out std_logic_Vector (7 downto 0)
           );
  end component;

  signal a : std_logic;
  signal b : std_logic_Vector (7 downto 0);

begin

     a  <= '0'
     , '1' after 10 ns
     , '0' after 20 ns
     , '1' after 30 ns
     , '0' after 40 ns
     , '1' after 50 ns
     , '0' after 60 ns
     , '1' after 70 ns
     , '0' after 80 ns
     , '1' after 90 ns;

    m: incrementer port map (a,b);

end bench;
```



This is the outcome of my test-bench.