CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #4

Due Date: Friday, September 30th 2011

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1. Create a VHDL circuit that has a single bit input (**a**) of type std_logic, and a 8-bit bus output (**b**) of type std_logic_vector. The 8-bit output bus should have the initial sate of zero. The circuit is to act as an "incrementer", that is; each time the input bit switches from low to high, the output should increment its value by one. So, the first time **a** goes high, **b** should output "00000001".
   a. Print a copy of your source code
   b. Create a test-bench for this circuit and print it, together with the resulting output wave-form that shows the accurate behavior of the circuit. Use Active HDL for this.