CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #5

Due Date: Friday, October 3rd 2011

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1. In the first code, the matrix (**x**) is initialized to those values, and its done only once; when the circuit is powered. In the second code, the matrix (**x**) is continuously being assigned those same values.

2. You can't assign values to an input port from inside the architecture block.

3.

parity encoder

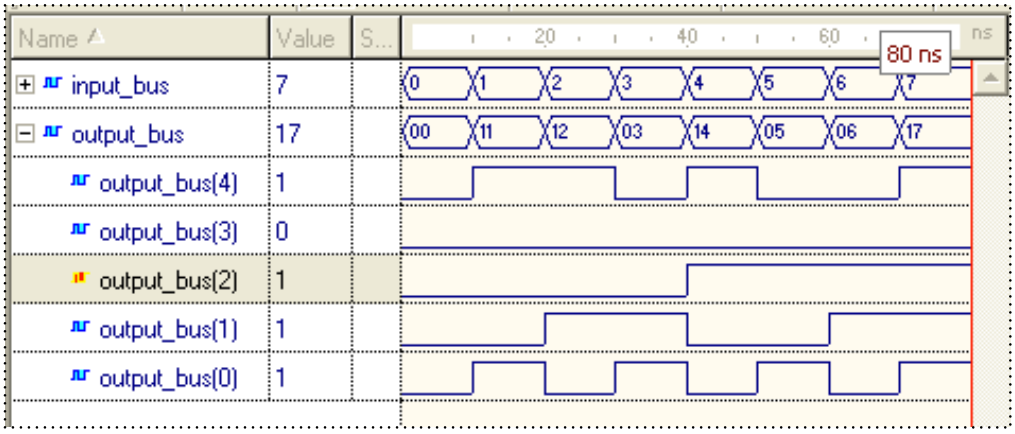
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity parity_encoder is
      port (input_bus  : in std_logic_vector(3 downto 0);
      output_bus : out std_logic_vector(4 downto 0)
      );
end entity;

architecture myarch of parity_encoder is
begin
      output_bus(4) <=
      input_bus(0) XOR input_bus(1)
      XOR input_bus(2) XOR input_bus(3);

      output_bus(0) <= input_bus(0);
      output_bus(1) <= input_bus(1);
      output_bus(2) <= input_bus(2);
      output_bus(3) <= input_bus(3);

end architecture;
```



4.

parity decoder

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity parity_decoder is
      port (input_bus  : in std_logic_vector(4 downto 0);
              parity_outcome : out std_logic
      );
end entity;

architecture myarch of parity_decoder is
      signal parity : std_logic;
begin
      parity <=
      input_bus(0) XOR input_bus(1)
      XOR input_bus(2) XOR input_bus(3);

      parity_outcome <= parity XOR input_bus(4);

end architecture;
```