CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #6

Due Date: Wednesday, October 5th 2011

1.

```
library ieee;
use ieee.std_logic_1164.all;

entity test is
end entity;

architecture myarch of test is
signal x: std_logic_vector (12512 downto 0):=(12507=>'0',others=>'1');
begin
end architecture;
```

2. Main code

```
LIBRARY ieee;
use ieee.std_logic_1164.all;

entity multiplier is
        port ( input : in std_logic_vector(7 downto 0);
        output : out  std_logic_vector(7 downto 0)
        );
end entity;

architecture myarch of multiplier is
        signal  bit_vec_inp     : bit_vector(7 downto 0);
        signal  bit_vec_outp    : bit_vector(7 downto 0);
begin

        bit_vec_inp    <= to_bitvector(input);
        bit_vec_outp   <= bit_vec_inp sll 1;
        output         <= to_stdlogicvector(bit_vec_outp);

end architecture;
```

Test-bench

```
LIBRARY ieee;
use ieee.std_logic_1164.all;

entity testmultiplier is
end;

architecture bench of testmultiplier is
  component multiplier
        port ( input : in std_logic_vector(7 downto 0);
        output : out  std_logic_vector(7 downto 0)
        );

  end component;

  signal input  : std_logic_vector(7 downto 0);
  signal output : std_logic_vector(7 downto 0);

begin
 input  <= "00000000"
 ,"00101000" after 10 ns
 ,"01010000" after 20 ns
 ,"01100000" after 30 ns
 ,"00110100" after 40 ns
 ,"00010101" after 50 ns
 ,"00100001" after 60 ns
 ,"00001100" after 70 ns
 ,"00111100" after 80 ns
 ,"00001110" after 90 ns;

    m: multiplier port map (input,output);

end bench;
```