CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #6

Due Date: Wednesday, October 5th 2011

Homework policy: If I see something unusual about your work, you can be sure I will ask you about it. If you are unable to explain it to me why you chose some implementation method I will have to consider your entire solution wrong. Now, what is my definition of "unusual work"? Well, things like suspicious parts of code that may have been copied from a website or chunks of your implementation that are very close to one of your colleagues. I really encourage communication amongst yourselves, and I want you guys to have a good time learning while doing these exercises... but please don't blindly copy code. If you really must, at least acknowledge your sources.

1. By changing only **"(some stuff in here)"** how would you initialize the signal x such that only the 5th element from the left is set to "zero", while all the other elements are set to "one". You do not have to compile this in Active HDL, but doing so is an easy way to see if your assignment is correct.

```
library ieee;
use ieee.std_logic_1164.all;

entity test is
end entity;

architecture myarch of test is
signal x: std_logic_vector (12512 downto 0) := "(some stuff in here)";
begin

end architecture;
```

2. Look at the following entity:

```
entity multiplier is
        port ( input : in std_logic_vector(7 downto 0);
        output : out  std_logic_vector(7 downto 0)
        );
end entity;
```

a) Using this entity, create a VHDL circuit that will multiply the circuit input (**inp**) by 2, and send the result to the circuit output (**outp**). You may **NOT** change the dimensions of the entity, which means you may not use the usual multiplier arithmetic operator. Also assume the input is going to be positive. **Hint:** If you are stuck, think about what multiplying by two means.

b) Create a test-bench that will test your circuit. Simulate your circuit in active HDL, but make sure each bus displays decimal values (right-click on a signal and edit its properties). Turn in a copy of your code, test-bench and waveforms.