CPE462 - VHDL: Simulation and Synthesis - Fall'11

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WESTERN NEW ENGLAND UNIVERSITY | WNE

Homework Assignment #8

Due Date: Friday, October 14th 2011

Question 1)

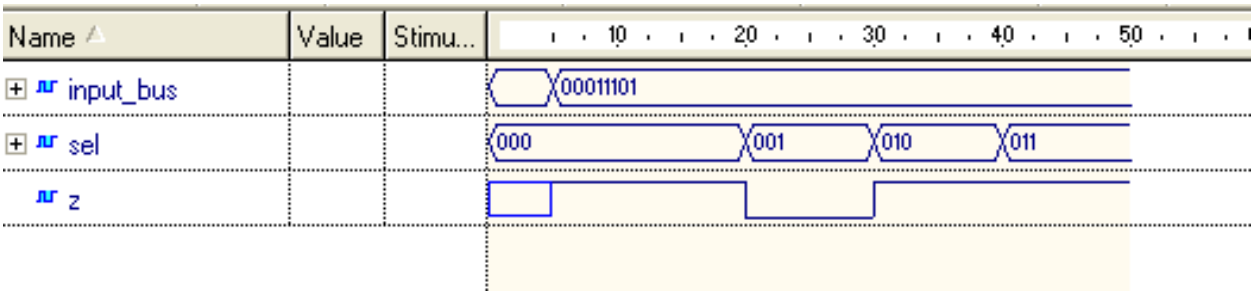
```
1  ------------------------------------------
2  LIBRARY ieee;
3  USE ieee.std_logic_1164.all;
4  USE ieee.std_logic_unsigned.all;
5  ------------------------------------------
6  ENTITY ALU IS
7     PORT (a, b: IN STD_LOGIC_VECTOR (7 DOWNTO 0);
8                sel: IN STD_LOGIC_VECTOR (3 DOWNTO 0);
9                cin: IN STD_LOGIC;
10               y: OUT STD_LOGIC_VECTOR (7 DOWNTO 0));
11 END ALU;
12 ------------------------------------------
13 ARCHITECTURE dataflow OF ALU IS
14    SIGNAL arith, logic: STD_LOGIC_VECTOR (7 DOWNTO 0);
15 BEGIN
16    ----- Arithmetic unit: ------
17    WITH sel(2 DOWNTO 0) SELECT
18       arith <=  a WHEN "000",
19                 a+1 WHEN "001",
20                 a-1 WHEN "010",
21                 b WHEN "011",
22                 b+1 WHEN "100",
23                  b-1 WHEN "101",
24                  a+b WHEN "110",
25                  a+b+cin WHEN OTHERS;
26    ----- Logic unit: -----------
27    WITH sel(2 DOWNTO 0) SELECT
28       logic <=  NOT a WHEN "000",
29                 NOT b WHEN "001",
30                 a AND b WHEN "010",
31                 a OR b WHEN "011",
32                 a NAND b WHEN "100",
33                 a NOR b WHEN "101",
34                 a XOR b WHEN "110",
35                 NOT (a XOR b) WHEN OTHERS;
36    -------- Mux: ---------------
37    WITH sel(3) SELECT
38       y <=  arith WHEN '0',
39             logic WHEN OTHERS;
40 END dataflow;
41 ------------------------------------------
```

Question 2)

Main code + test-bench with a single bit input

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity generic_mux is
        generic (n: integer := 3);
        port (input_bus: in std_logic_vector( (2**n)-1 downto 0 );
        sel : in std_logic_vector(n-1 downto 0);
        z : out std_logic);
end entity;

architecture myarch of generic_mux is

begin
 z <= input_bus(conv_integer(sel)) when (conv_integer(sel)<n+2) else ('Z');

end architecture;
```

```
library ieee;
use ieee.std_logic_1164.all;

entity test_generic_mux is
end;

architecture bench of test_generic_mux is
  constant n : positive := 3;
  component generic_mux
        generic (n: integer := n);
        port (input_bus: in std_logic_vector( (2**n)-1 downto 0);
        sel : in std_logic_vector(n-1 downto 0);
        z : out std_logic);
  end component;

  signal input_bus  : std_logic_vector( (2**n)-1 downto 0);
  signal sel : std_logic_vector(n-1 downto 0);
  signal z : std_logic;

begin

 input_bus   <= "XXXX" , "01X1" after 5 ns;
 sel <= "00", "01" after 20ns, "10" after 30ns, "11" after 40ns;

 m: generic_mux  generic map(n) port map (input_bus,sel,z);

end bench;
```


Name
Value
Stimu...
10
20
30
40
50
input_bus
00011101
sel
000
001
010
011
z