CPE462 - VHDL: Simulation and Synthesis - Fall'11

Prof. Nuno Alves (nalves@wne.edu), College of Engineering

Homework Assignment #9

Due Date: Monday, October 17th 2011

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## Question 1)

```
library ieee;
use ieee.std_logic_1164.all;

entity priority_encoder is
        signal input  : std_logic_vector (7 downto 0);
        signal output : std_logic_vector (2 downto 0);
end entity;

architecture myarch of priority_encoder is
begin

output <=
                "111" when (input(7)='1')  else
                "110" when (input(6)='1')  else
                "101" when (input(5)='1')  else
                "100" when (input(4)='1')  else
                "011" when (input(3)='1')  else
                "010" when (input(2)='1')  else
                "001" when (input(1)='1')  else
                "000" when (input(0)='1')  else
                "ZZZ";

end architecture;
```

## Question 2)

```
library ieee;
use ieee.std_logic_1164.all;

entity q2 is
        port( a,b  : in integer range -127 to 127;
              x,y  : out integer);
end entity;

architecture myarch of q2 is
begin

x <= a * b;
y <= a / 2;

end architecture;
```

**Question 3)**

Main-code:

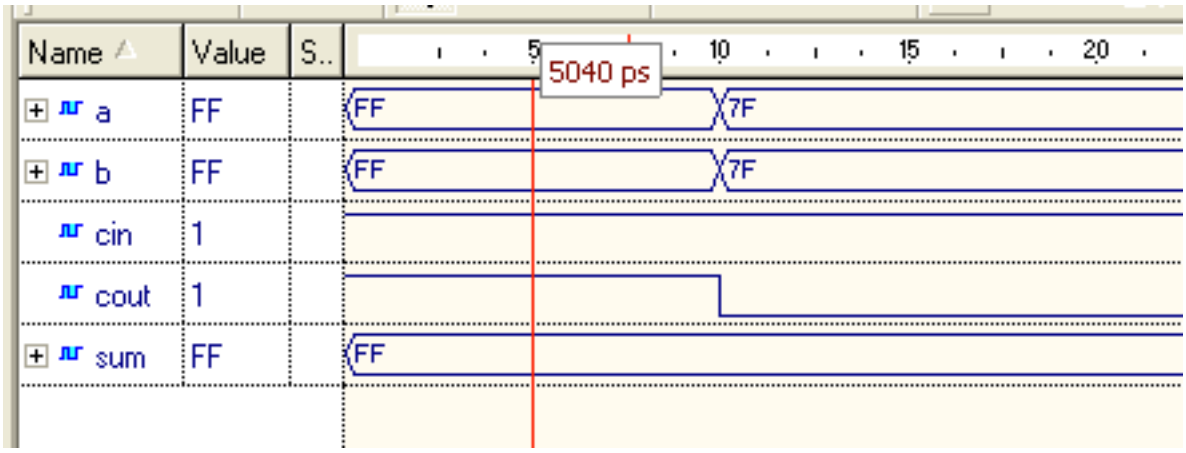
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity q3 is
        port( a,b  : in std_logic_vector(7 downto 0);
        cin : in std_logic;
        cout : out std_logic;
        sum : out std_logic_vector(7 downto 0)
        );
end entity;

architecture myarch of q3 is
begin

        b1: block
        signal temp_a : std_logic_vector (8 downto 0);
        signal temp_b : std_logic_vector (8 downto 0);
        signal temp_sum : std_logic_vector (8 downto 0);
        begin
           temp_a <= '0' & a;
           temp_b <= '0' & b;
           temp_sum <= temp_a+temp_b+cin;

           cout <= '1' when (temp_sum(8)='1')  else '0';
           sum <=  temp_sum(7 downto 0);
        end block;
end architecture;
```



Test-bench:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

entity test_q3 is
end;

architecture bench of test_q3 is
  component q3
        port( a,b  : in std_logic_vector(7 downto 0);
        cin : in std_logic;
        cout : out std_logic;
        sum : out std_logic_vector(7 downto 0)
        );
  end component;

signal a,b  : std_logic_vector(7 downto 0);
signal cin  : std_logic;
signal cout : std_logic;
signal sum  : std_logic_vector(7 downto 0);

begin
 a  <= "11111111",
 "01111111" after 10 ns;

 b  <= "11111111",
 "01111111" after 10 ns;

 cin <= '1';
 m: q3 port map (a,b,cin,cout,sum);

end bench;
```