CPE462 - VHDL: Simulation and Synthesis - Fall'11

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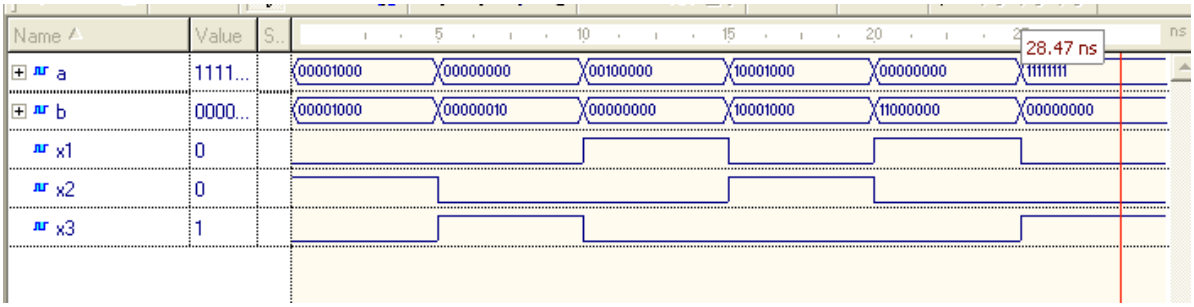
HW #11 Solutions

Question #1:



```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity compare is
        port (a,b : in std_logic_vector(7 downto 0);
        sel : in std_logic;
        x1,x2,x3 : out std_logic);
end entity;


architecture myarch of compare is
        signal unsigned_a,unsigned_b : unsigned (7 downto 0);
        signal signed_a,signed_b : signed (7 downto 0);
        signal unsigned_x1,unsigned_x2,unsigned_x3 : std_logic;
        signal signed_x1,signed_x2,signed_x3 : std_logic;
        signal integer_a, integer_b : integer;
begin

        unsigned_a <= unsigned(a);
        unsigned_b <= unsigned(b);

        signed_a <= signed(a);
        signed_b <= signed(b);

        -- is a and b equal?
        unsigned_x2 <= '1' when unsigned_a=unsigned_b else
                  '0';
        signed_x2 <= '1' when signed_a=signed_b else
                '0';

        -- is a>b
        unsigned_x1 <= '1' when unsigned_a>unsigned_b else
                '0';
        signed_x1 <= '1' when signed_a>signed_b else
                '0';

        -- is a<b
        unsigned_x3 <= '1' when unsigned_a<unsigned_b else
                  '0';
        signed_x3 <= '1' when signed_a<signed_b else
                  '0';

        --route the appropriate signal to an the output using a mux
        x1 <= unsigned_x1 when sel='0' else
                signed_x1;
        x2 <= unsigned_x2 when sel='0' else
                signed_x2;
        x3 <= unsigned_x3 when sel='0' else
                signed_x3;
end architecture;
```