CPE462 - VHDL: Simulation and Synthesis - Fall'11

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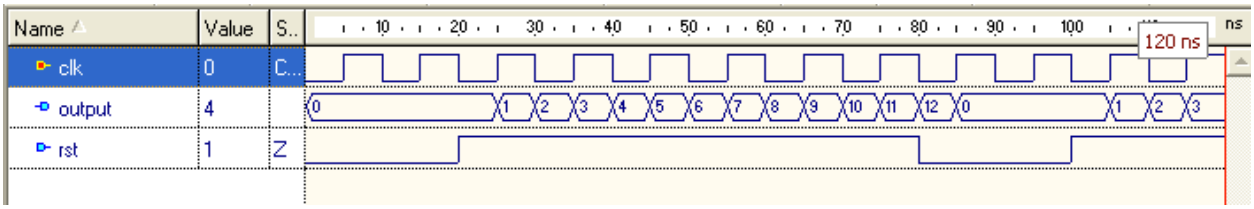
Homework Assignment #12

Due Date: Friday, October 28th 2011

Question #1

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity edgecounter is
        port (clk, rst : in std_logic;
        output : out integer);
end entity;

architecture myarch of edgecounter is
begin
        process(clk)
                variable counter : integer ;
        begin
                if (clk'event) then
                        counter := counter + 1;
                end if;

                if (rst='0') then counter :=0; end if;

                output<=counter;
        end process;

end architecture;
```



Question #2

```
library ieee;
use ieee.std_logic_1164.all;

entity counter is
        port (clk, rst : in std_logic;
        digit : out integer range 3 to 11);
end entity;

architecture myarch of counter is
begin
        process(clk)
                variable temp : integer range 3 to 12;
        begin

                if (rst = '1') then temp := 6; end if;

                if (clk'event and clk='1') then
                        temp := temp + 1;
                        if (temp=12) then temp:=3; end if;
                        digit<=temp;
                end if;

        end process;

end architecture;
```