CPE462 - VHDL: Simulation and Synthesis - Fall'11

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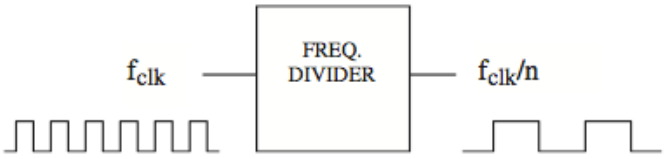
Homework Assignment #15

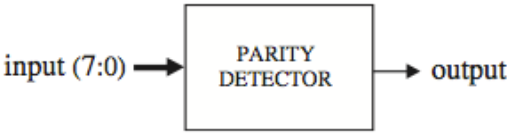
Due Date: Wednesday, November 16 2011

Homework policy: If I see something unusual about your work, you can be sure I will ask you about it. If you are unable to explain it to me why you chose some implementation method I will have to consider your entire solution wrong. Now, what is my definition of "unusual work"? Well, things like suspicious parts of code that may have been copied from a website or chunks of your implementation that are very close to one of your colleagues. I really encourage communication amongst yourselves, and I want you guys to have a good time learning while doing these exercises... but please don't blindly copy code. If you really must, at least acknowledge your sources.

1. Write a VHDL code for a circuit capable of dividing the frequency of an input clock signal by an integer n. The code should be **generic**; that is, n should be defined using the GENERIC statement.



2. The following image shows the top-level diagram of a parity detector. This particular input vector has eight bits. The output must be '0' when the number of '1's in the input vector is even, or '1' otherwise. Write a **generic sequential** code for this circuit.



3. Consider the DFF with asynchronous reset. Below are several codes for that circuit. Examine each of them and determine whether they should work properly. Briefly explain your answers.

```
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LIBRARY ieee;
USE ieee.std_logic_1164.all;
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ENTITY dff IS
   PORT ( d, clk, rst: IN BIT;
          q: OUT BIT);
END dff;
----- Solution 1 --------------------
ARCHITECTURE arch1 OF dff IS
BEGIN
   PROCESS (clk, rst)
   BEGIN
      IF (rst='1') THEN
         q <= '0';
      ELSIF (clk'EVENT AND clk='1') THEN
         q <= d;
      END IF;
   END PROCESS;
END arch1;
----- Solution 2 --------------------
ARCHITECTURE arch2 OF dff IS
BEGIN
   PROCESS (clk)
   BEGIN
      IF (rst='1') THEN
         q <= '0';
      ELSIF (clk'EVENT AND clk='1') THEN
         q <= d;
      END IF;
   END PROCESS;
END arch2;
----- Solution 3 --------------------
ARCHITECTURE arch3 OF dff IS
BEGIN
   PROCESS (clk)
   BEGIN
      IF (rst='1') THEN
         q <= '0';
      ELSIF (clk'EVENT) THEN
         q <= d;
      END IF;
   END PROCESS;
END arch3;
```

```
----- Solution 4 ---------------------
ARCHITECTURE arch4 OF dff IS
BEGIN
   PROCESS (clk)
   BEGIN
      IF (rst='1') THEN
         q <= '0';
      ELSIF (clk='1') THEN
         q <= d;
      END IF;
   END PROCESS;
END arch4;
----- Solution 5 ---------------------
ARCHITECTURE arch5 OF dff IS
BEGIN
   PROCESS (clk, rst, d)
   BEGIN
      IF (rst='1') THEN
         q <= '0';
      ELSIF (clk='1') THEN
         q <= d;
      END IF;
   END PROCESS;
END arch5;
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```

Extra-Credit:

4. This is a thinking question where no code needs to be written.
   a) How would you approach the opposite of problem 1 in VHDL. That is, say that we want to multiply the clock frequency by n.
   b) How would you create a faster frequency from an oscillator in a physical circuit?