CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #17

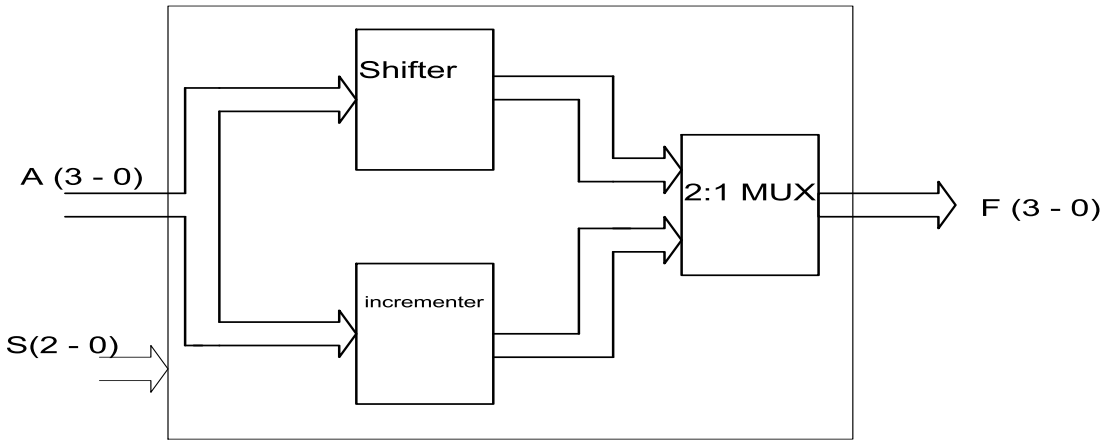
Due Date: Monday, December 05 2011

Question 1 - Create a circuit in VHDL that will implement the following functionality:

- There is one 4-bit data input 'A' that goes to both the shifter and the incrementer.
- The outputs of the shifter and incrementer are 4-bits wide, and 'F' is 4 bits.
- There is also a 3-bit control input S(2 – 0). S(1) and S(0) control the functions of the shifter and incrementer, as described below.
- S(2) controls the 4-wide 2:1 MUX that provides the output. If S(2) = 0 the shifter output goes to 'F'; if S(2) = 1 then incrementer output goes to 'F'.

Requirements:

1) Shifter, Incrementer and the 2:1 MUX **must** be three different components. Print out each of these three components.
2) Use a package to declare these three components. Print out the package VHDL file.
3) Set all inputs/outputs on your wave-form to be displayed in binary, simulate your circuit for 80 ns and fit the entire waveform on the screen (use the fit-to-screen option), and take a screenshot.
4) Take a screenshot of your ActiveHDL environment setup, which shows all used files with a green check sign next to it. You need to use 5 files in your design (1 top_level design file, 3 component files, and 1 package file).



S(1)	S(0)	Shifter function	Incrementer function
0	0	A shift right 1 bit	A + 1
0	1	A shift left 2 bits	A - 1
1	0	A (unchanged)	A + 2
1	1	Reverse order of bits *	High Impedance

Example: If A="1Z0X", the output of the shifter function should be "X0Z1".

Question 2 - Create a generic component in VHDL that implements the majority function, or the majority gate. Demonstrate its functionality with 3 inputs and also with 5 inputs. If you do not remember, the majority gate is a function from n inputs to one output. The value of the operation is false when n/2 or more arguments are false, and true otherwise.