CPE462 - VHDL: Simulation and Synthesis - Fall'11

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Homework Assignment #18

Due Date: Monday, December 12 2011

Question 1

Package

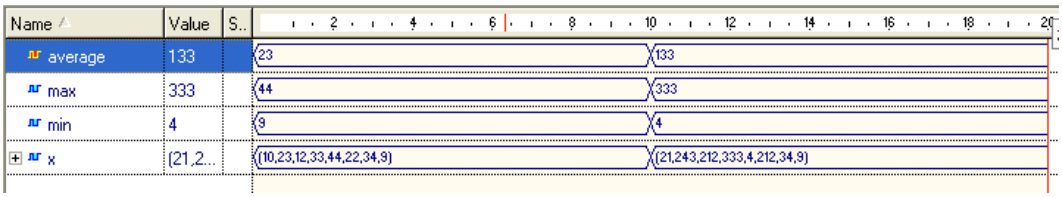
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

PACKAGE my_package IS

type matrix is array (7 downto 0) of integer;
procedure calculate (signal x: in matrix ; signal max, min, average : out
integer);

END PACKAGE;

package body my_package IS

 procedure calculate (signal x: in matrix ; signal max, min, average : out
integer) is
 variable tempmax : integer := x(0);
 variable tempmin : integer := x(0);
 variable sum : integer := 0;
 begin

        for i in 0 to 7 loop
                sum := sum + x(i);
                if (x(i) > tempmax) then tempmax := x(i); end if;
                if (x(i) < tempmin) then tempmin := x(i); end if;
        end loop;

        max <= tempmax;
        min <= tempmin;
        average <= sum / 8;

 end procedure;
end package body;
```

Main Program

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE work.my_package.all;

entity topLevel is
        port (  x : in matrix;
                        max, min, average : out integer);
end entity;

architecture STRUCTURE of topLevel is

begin
 calculate (x,max,min,average);

end architecture;
```

Test-bench

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
USE work.my_package.all;

entity testadder is
end;

architecture bench of testadder is
  component topLevel is
        port (  x : in matrix;
                        max, min, average : out integer);
        end component;

  signal x : matrix;
  signal max, min, average : integer;

begin
 x   <= (10,23,12,33,44,22,34,9), (21,243,212,333,4,212,34,9) after 10ns ;

 m: topLevel port map (x,max,min,average);

end bench;
```



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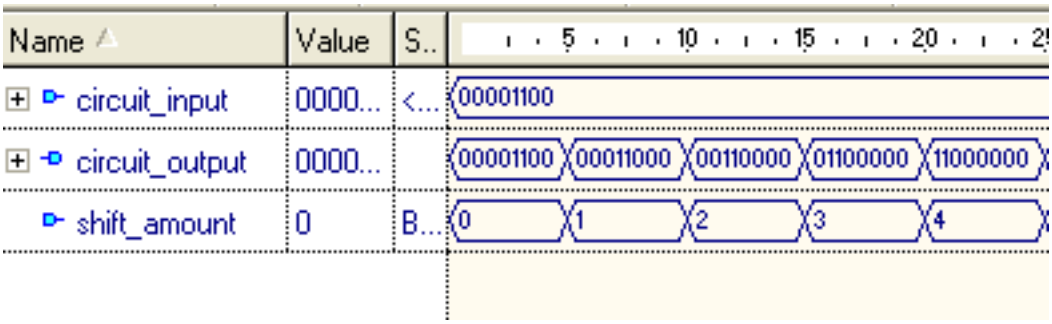
Question 2 -

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity main_block is
port (circuit_input : in integer range 0 to 255;
         circuit_output : out integer range 0 to 255
);
end entity;

architecture myarch of main_block is

function "NOT" (a : integer) return integer is
variable temp1 : std_logic_vector (7 downto 0);
begin
   temp1 := conv_std_logic_vector(a,8);
   temp1 := NOT(temp1);
   return conv_integer(temp1);

end function;

begin
        circuit_output<= NOT(circuit_input);
end architecture;
```

Question 3 -



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity main_block is
port ( circuit_input : in std_logic_vector (7 downto 0);
           shift_amount : in integer;
       circuit_output : out std_logic_vector (7 downto 0)
);
end entity;

architecture myarch of main_block is

function shiftit (a : std_logic_vector; b: integer) return std_logic_vector
is
variable temp1 : bit_vector (7 downto 0);
begin
   temp1 := to_bitvector(a);
   temp1 := temp1 sll b;
   return to_stdlogicvector(temp1);
end function;

begin

        circuit_output<=shiftit (circuit_input,shift_amount);

end architecture;
```