CPE 462
VHDL: Simulation and Synthesis

Topic #02 - b) Review of Sequential Logic

What is sequential logic

Sequential logic is a type of logic circuit... whose output depends not only on the present input but also on the history of the input.

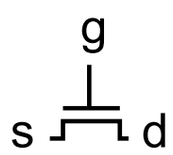
In combinational logic, the output is a function of, and only of, the present input.

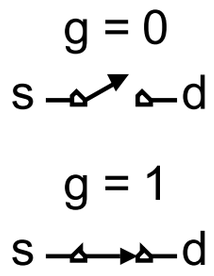
In other words, sequential logic has state (memory) while combinational logic does not.

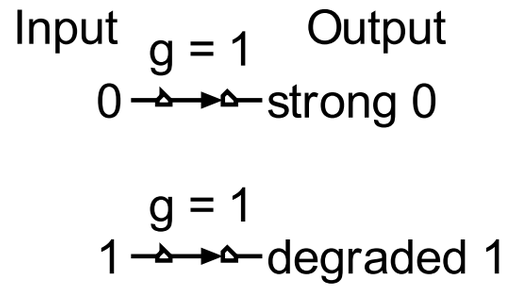
Sequential logic is used to construct some types of computer memory storage elements, and finite state machines.

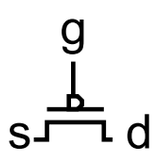
Quick review on transmission gates

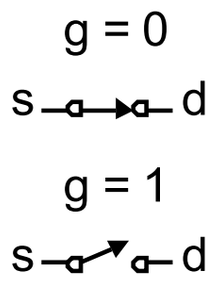
Transistors can be used as switches

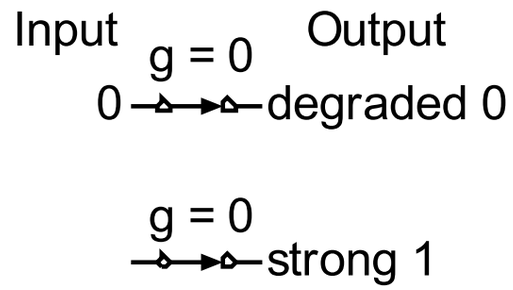




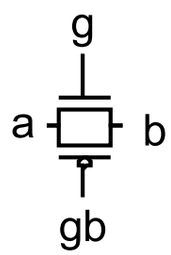


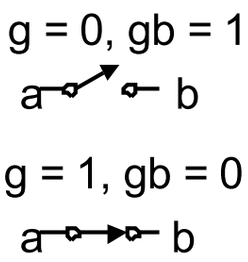


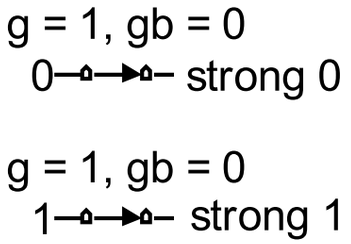




Transmission gates pass strong 1's and 0's







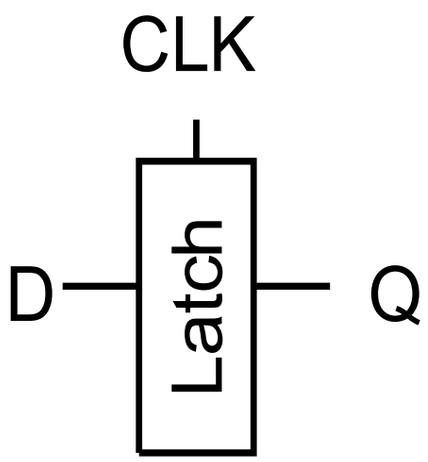
Basic D-Latch

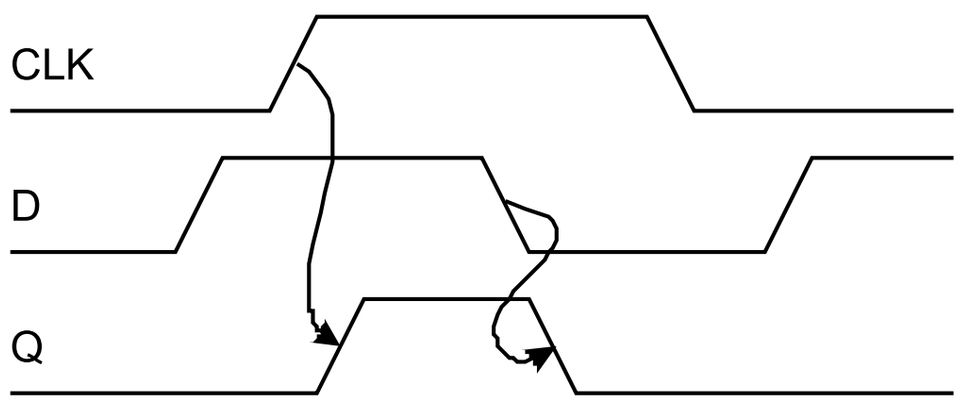
When CLK = 1

- Latch is transparent. This means...
- ... Q follows D (a buffer with a delay)

When CLK = 0

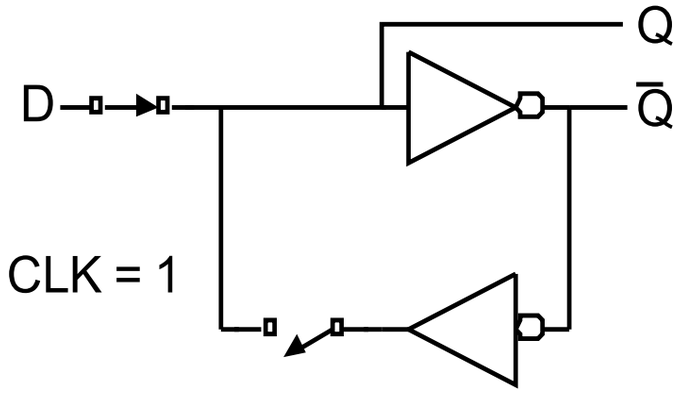
- Latch is opaque
- Q holds its last value independent of D

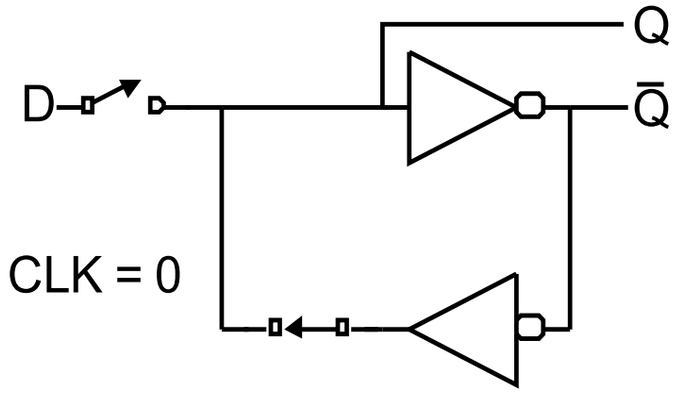


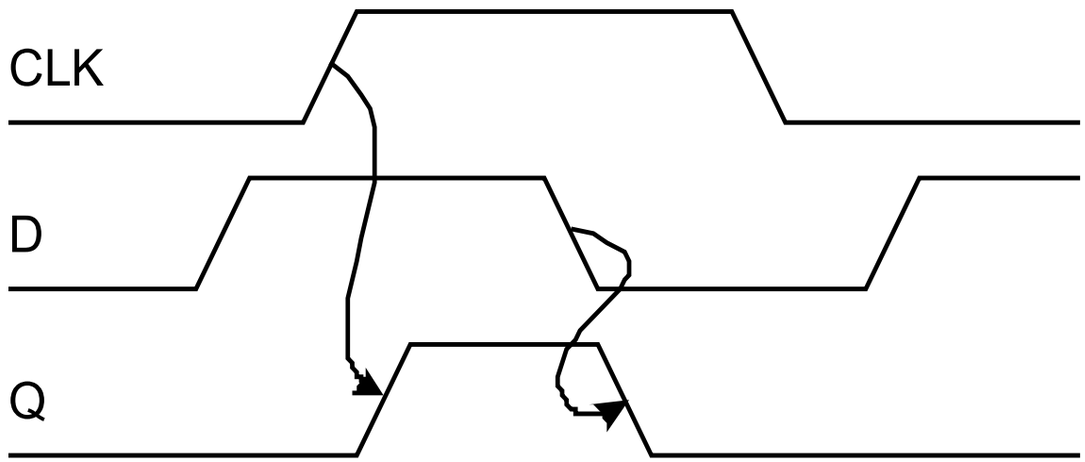


D-Latch operation

Inputs		Outputs		
Clock	D	Q	~Q	Comment
0	X	Qprev	~Qprev	No change
1	0	0	1	Reset
1	1	1	0	Set

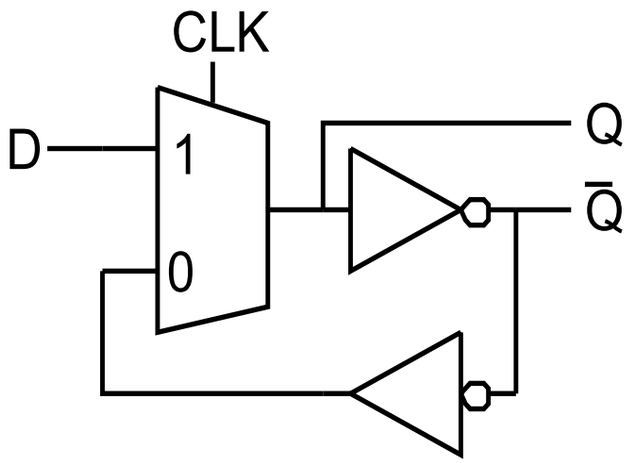




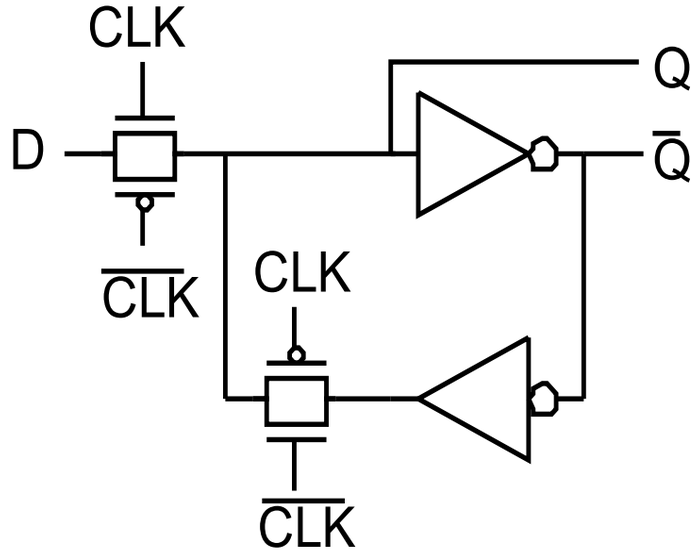


Two D-Latch designs

Multiplexer chooses D or old Q



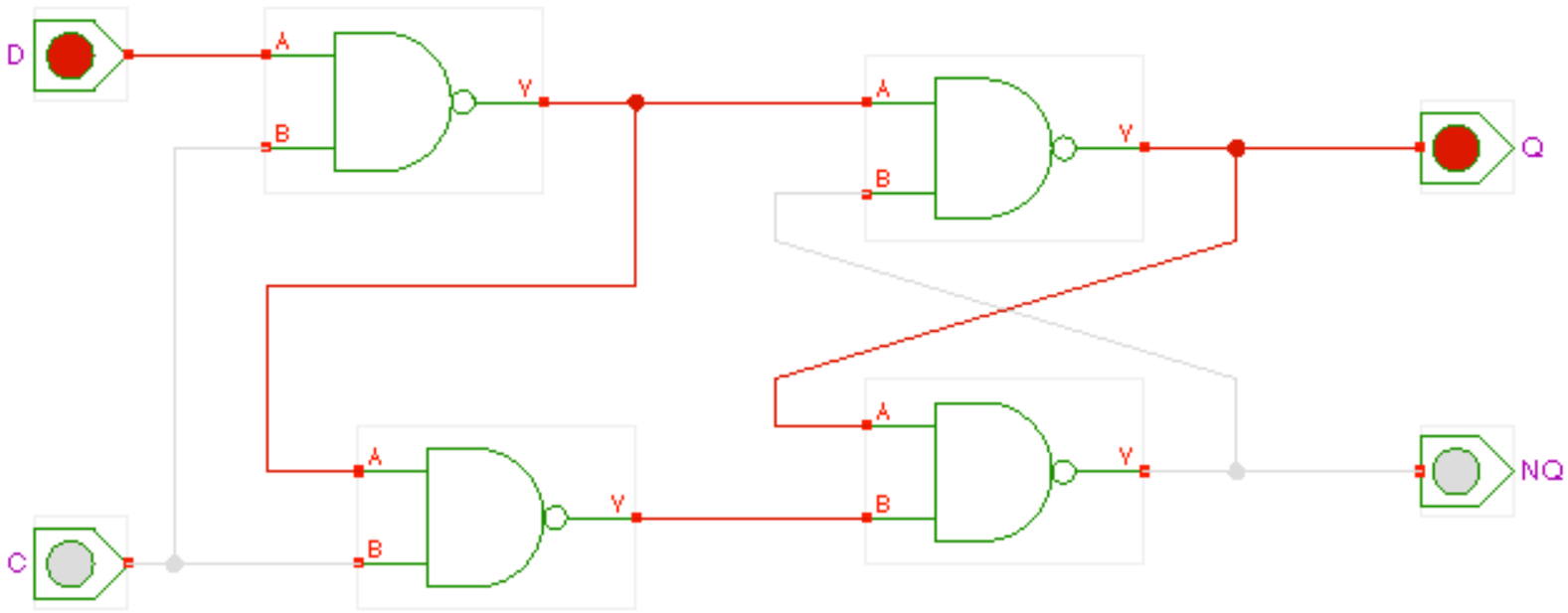
...With a MUX



...With transmission gates

Another D-Latch design

... D-Latch implemented with NAND gates

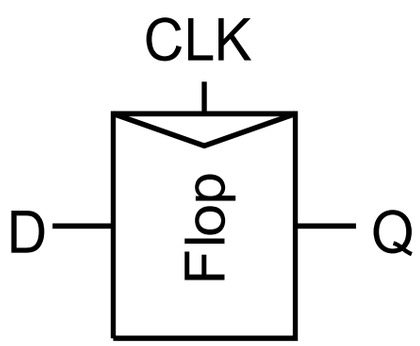


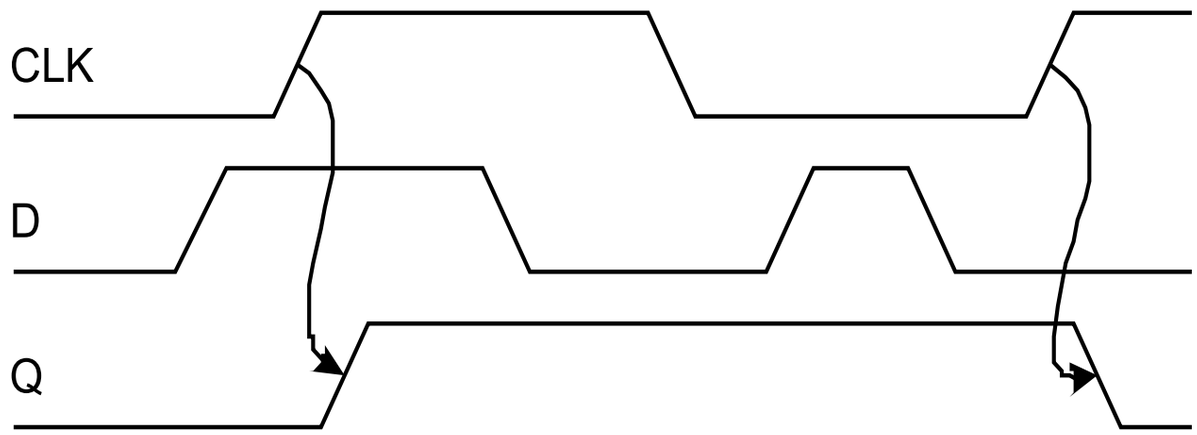
I **highly** recommend the following website, which contains simulations of sequential elements:

http://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/16-flipflops/20-dlatch/dlatch.html

D-Flip Flop

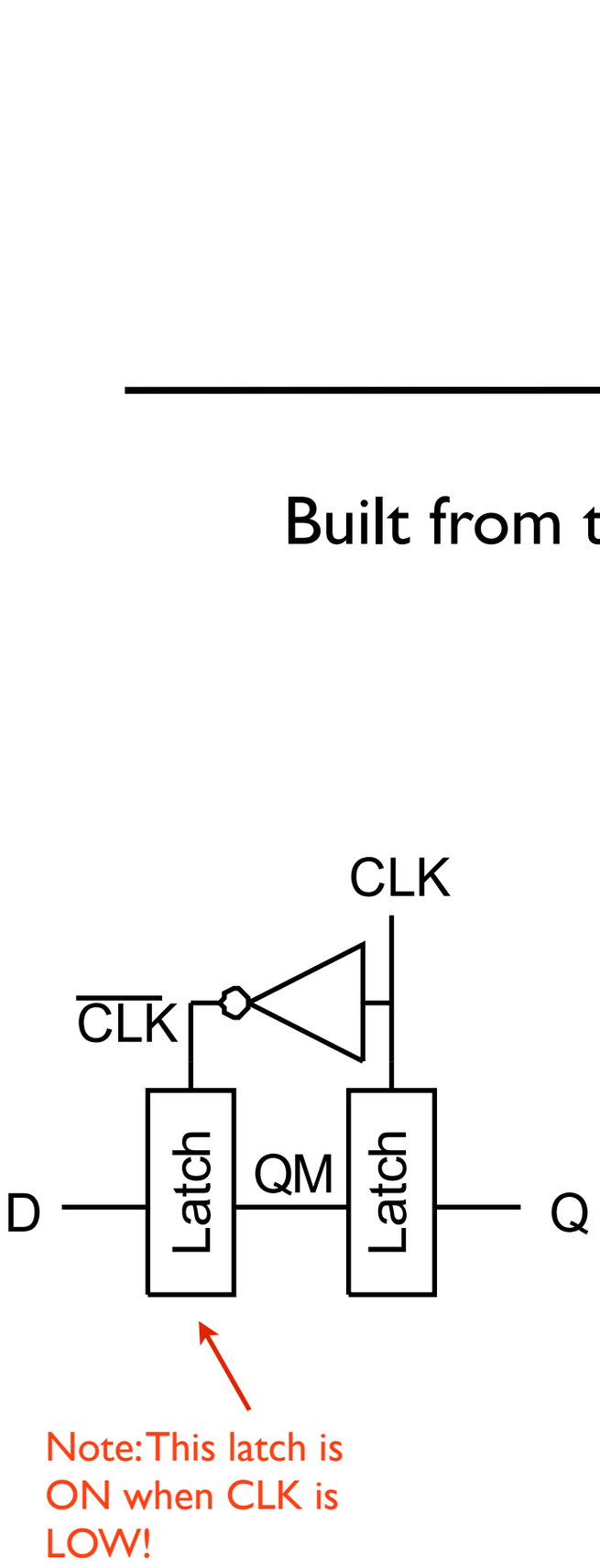
- **Only when CLK rises**, D is copied to Q
- At all other times, Q holds its value
- a.k.a. positive edge-triggered flip-flop, master-slave flip-flop



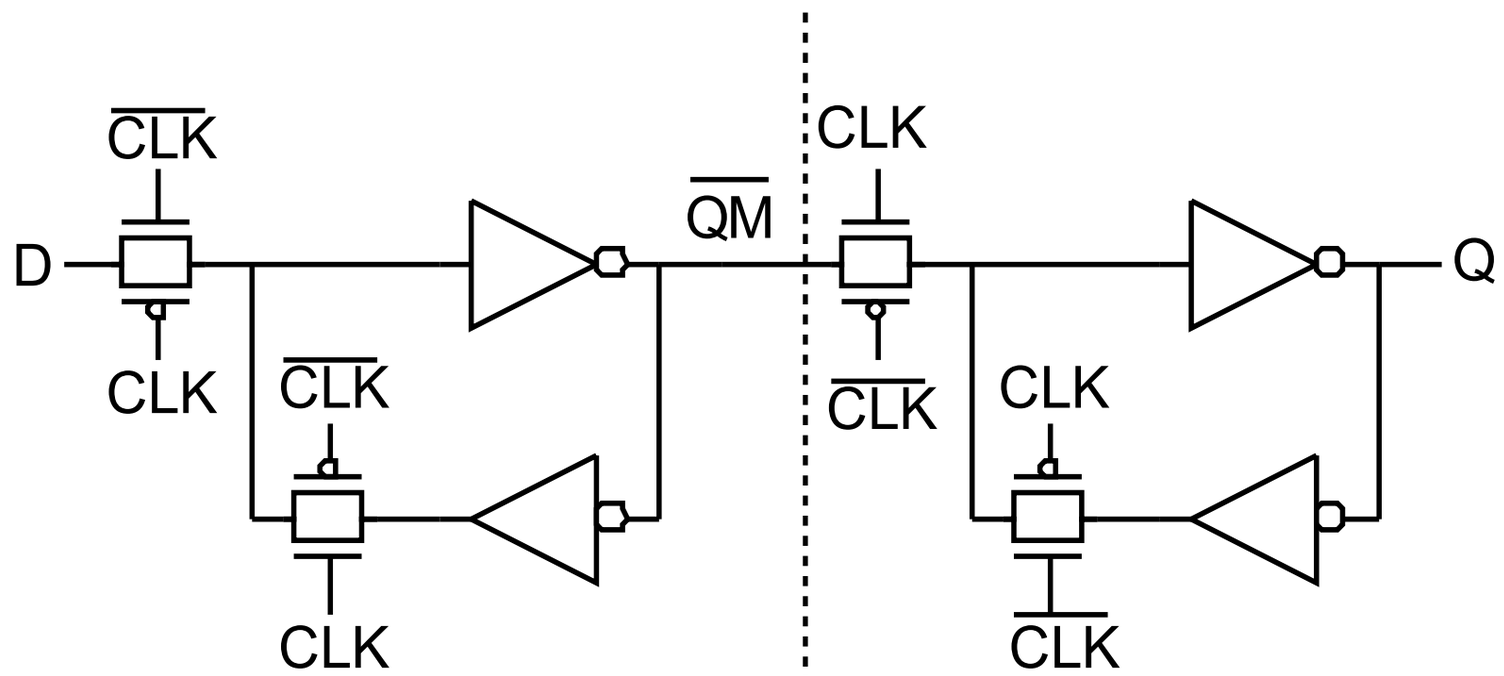


D-Flip Flop design

Built from two D latches (one is master, other is the slave)



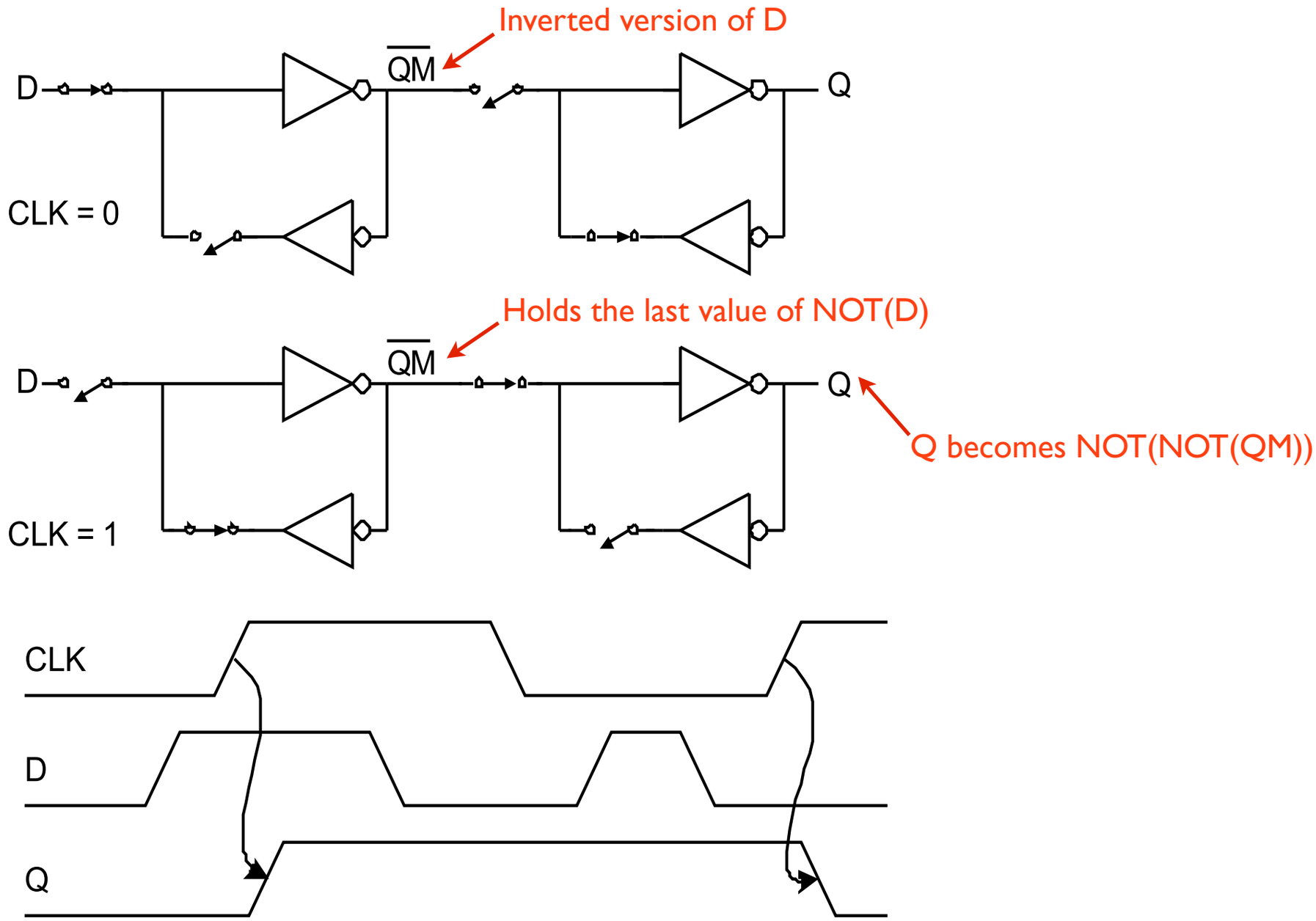
Note: This latch is ON when CLK is LOW!



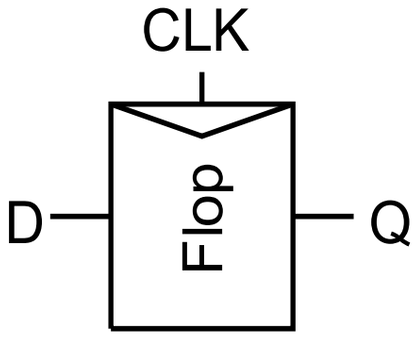
"Negative level-sensitive" latch

"Positive level-sensitive" latch

D-Flip Flop operation

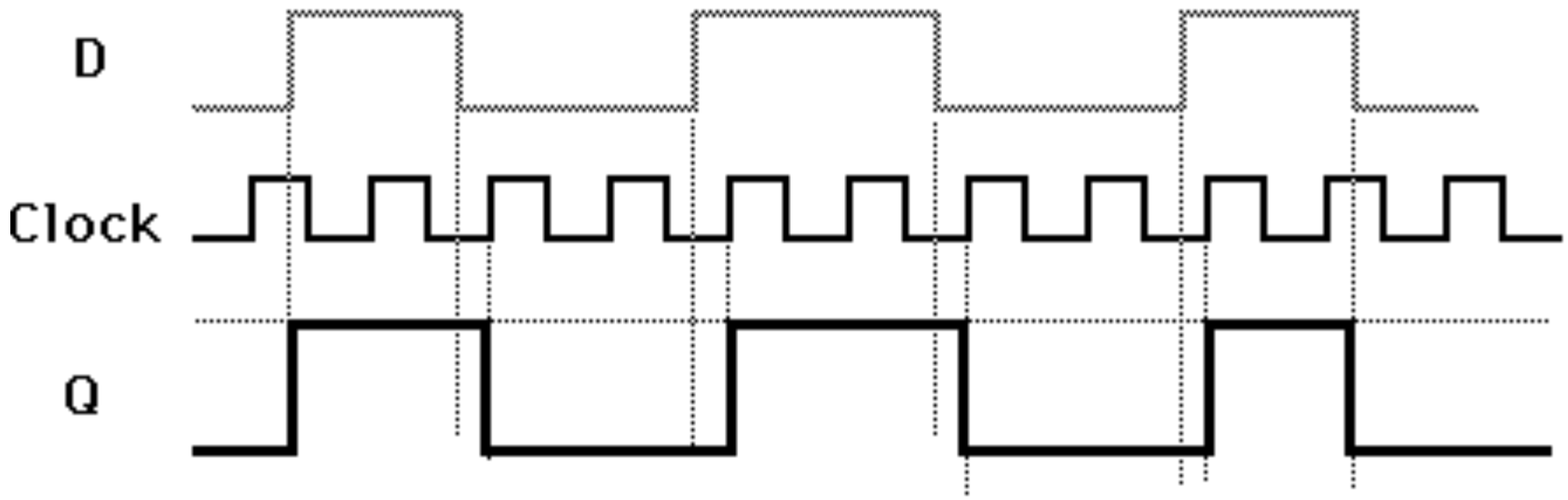


D-FF example output



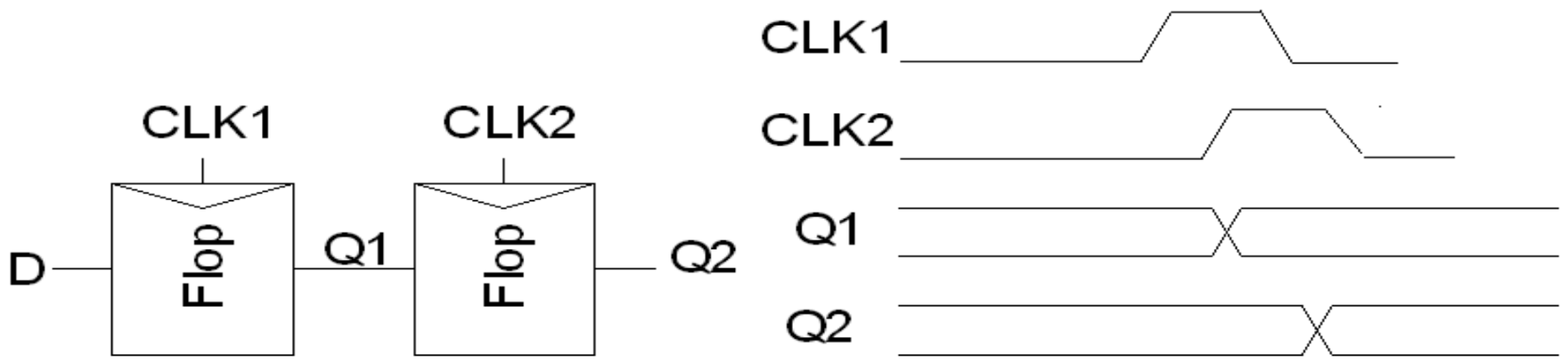
The D-FF tries to follow the input D but cannot make the required transitions unless it is enabled by the clock.

Note that if the clock is low when a transition in D occurs, the tracking transition in Q occurs at the next upward transition of the clock.



Final remarks on D-FF

- The D flip-flop is the most common flip-flop in use today
- We will probably only use this type of FF in this class
- Flip-flops are prone to race conditions
- Example: Due to clock skew, the second FF fires early and sees first flip-flop change and captures its result

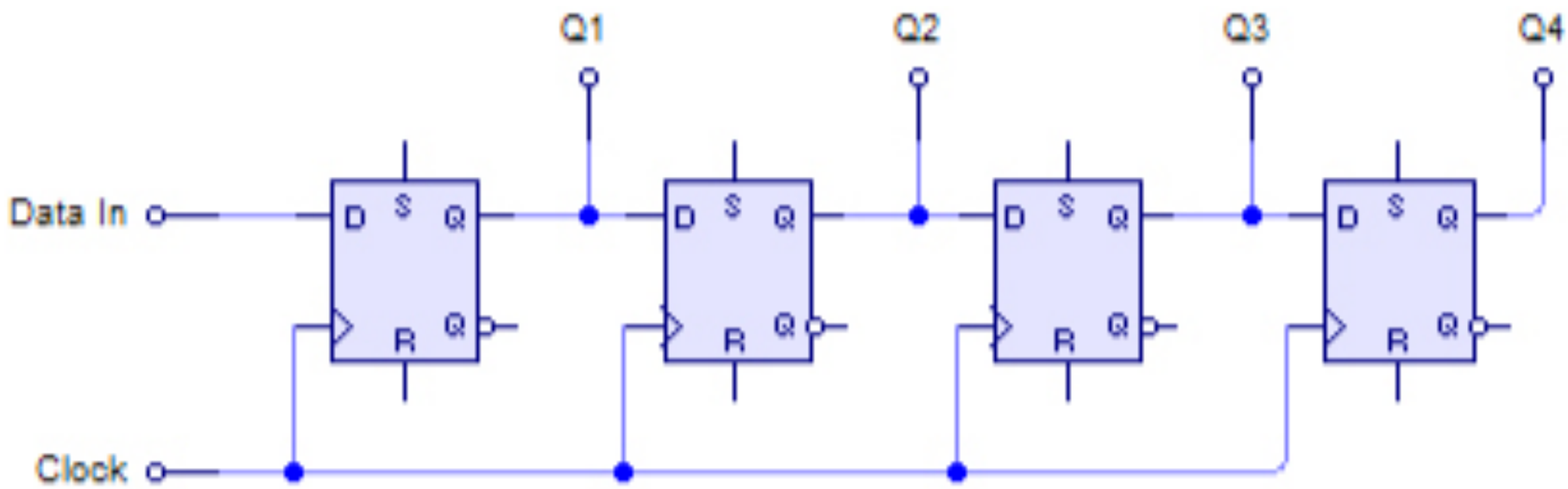


Some examples of FF usage

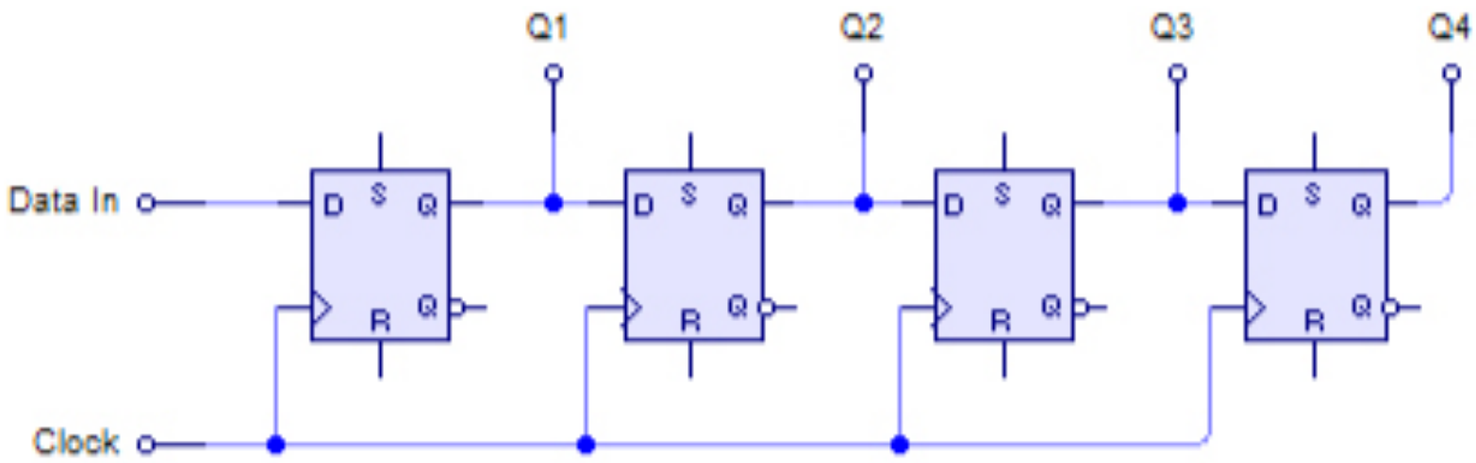
Serial-in, parallel-out (SIPO) shift register

- SIPO registers are attached to the output of microprocessors when more output pins are required than are available

- Allows several devices to be controlled using only two or three pins

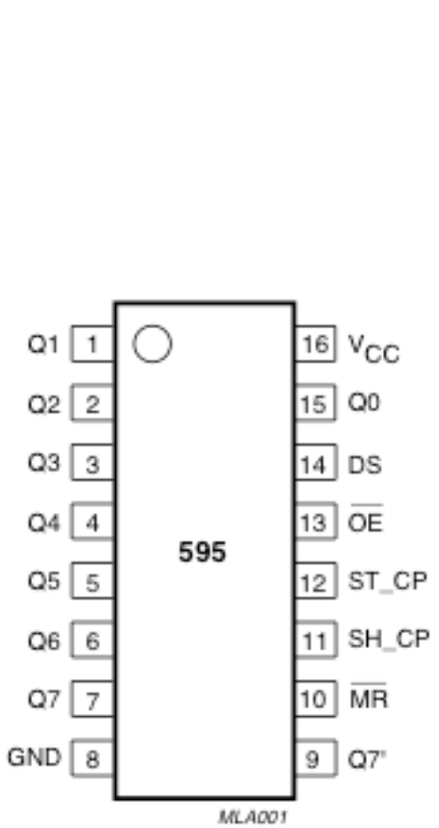


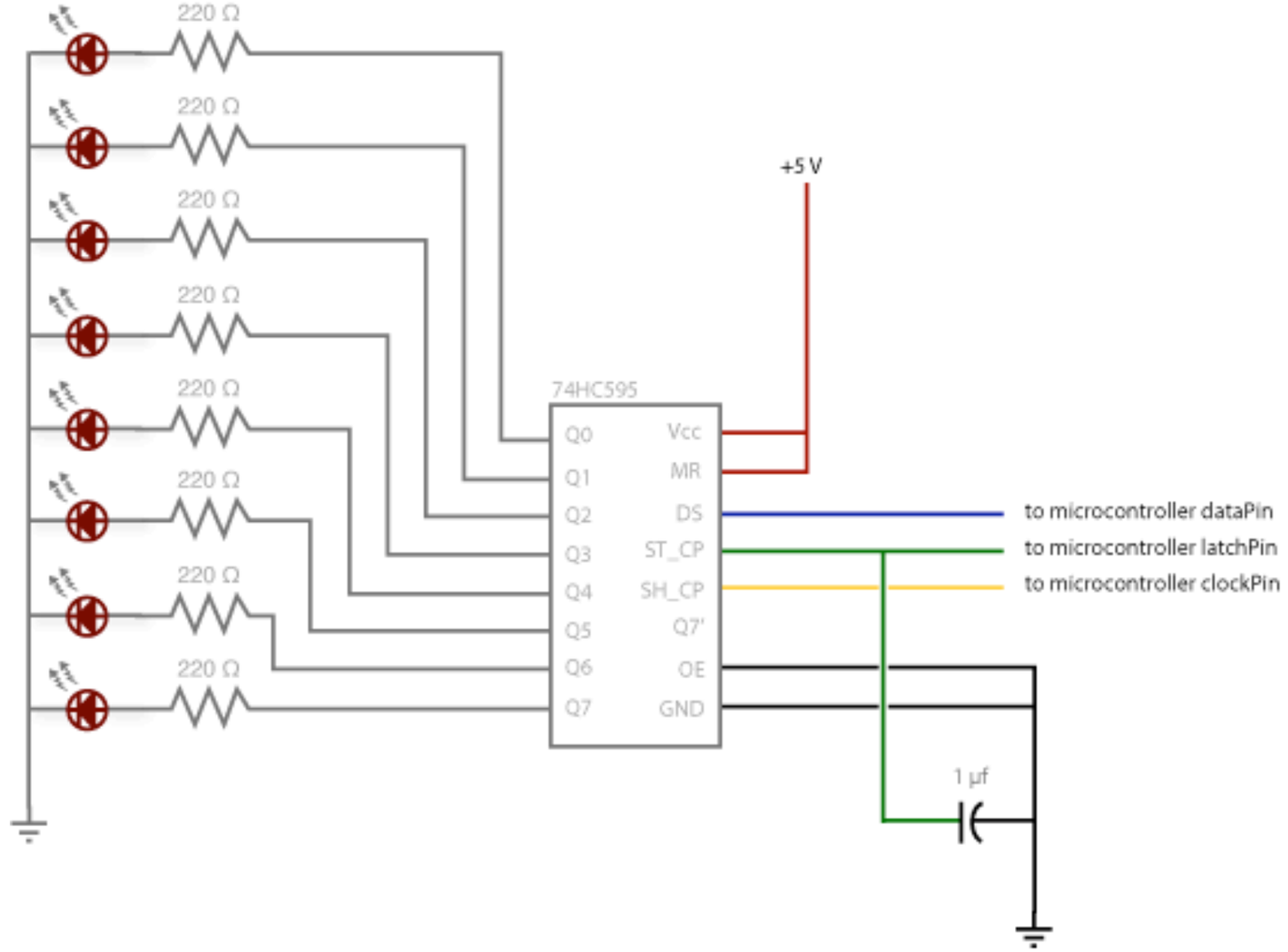
We want a light to be ON at Q1 and Q4!



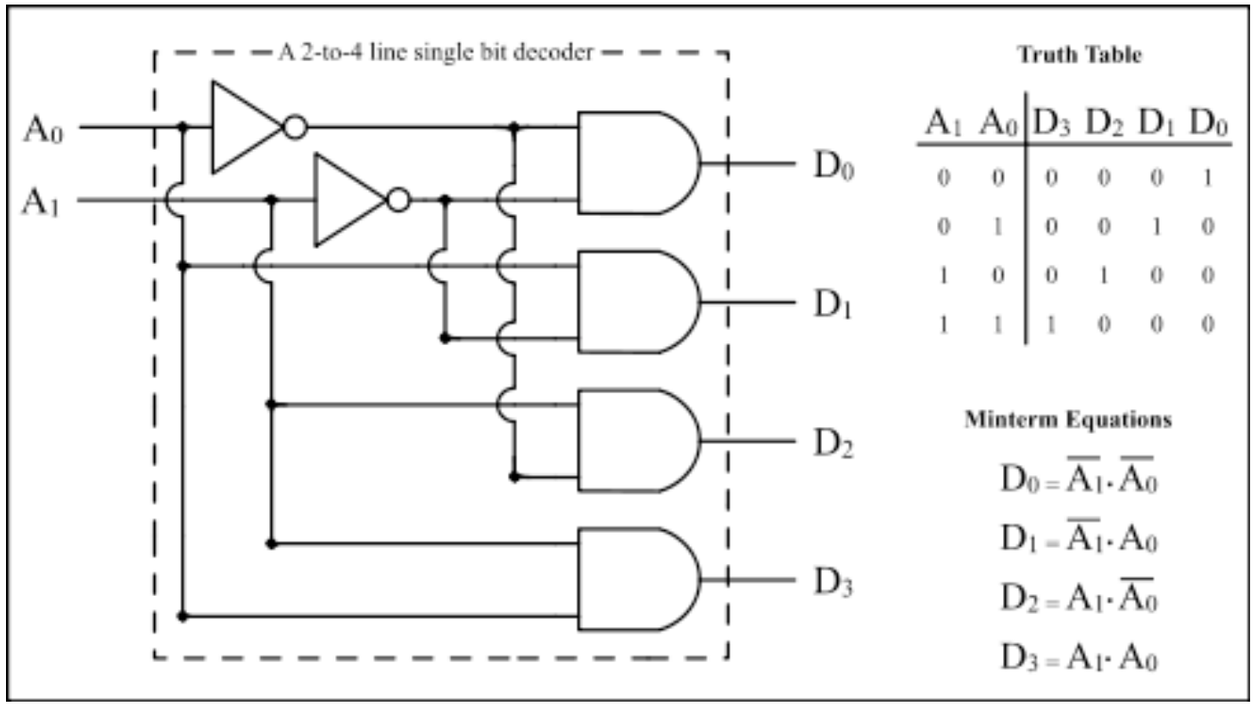
Data In	Clock	Q1	Q2	Q3	Q4
1	0	X	X	X	X
1	1	1	X	X	X
0	0	1	X	X	X
0	1	0	1	X	X
0	0	0	0	1	X
0	1	0	0	1	X

Example of a shift-register

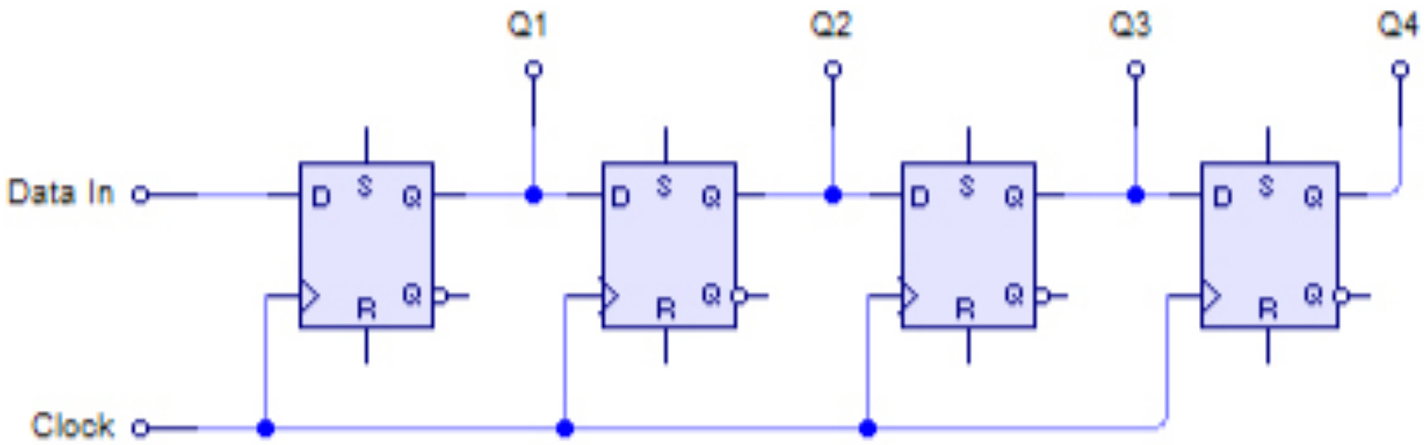




Difference between a shift register and a single-bit decoder?



Suppose the outputs of both the shift-register and the decoder are feeding LEDs...



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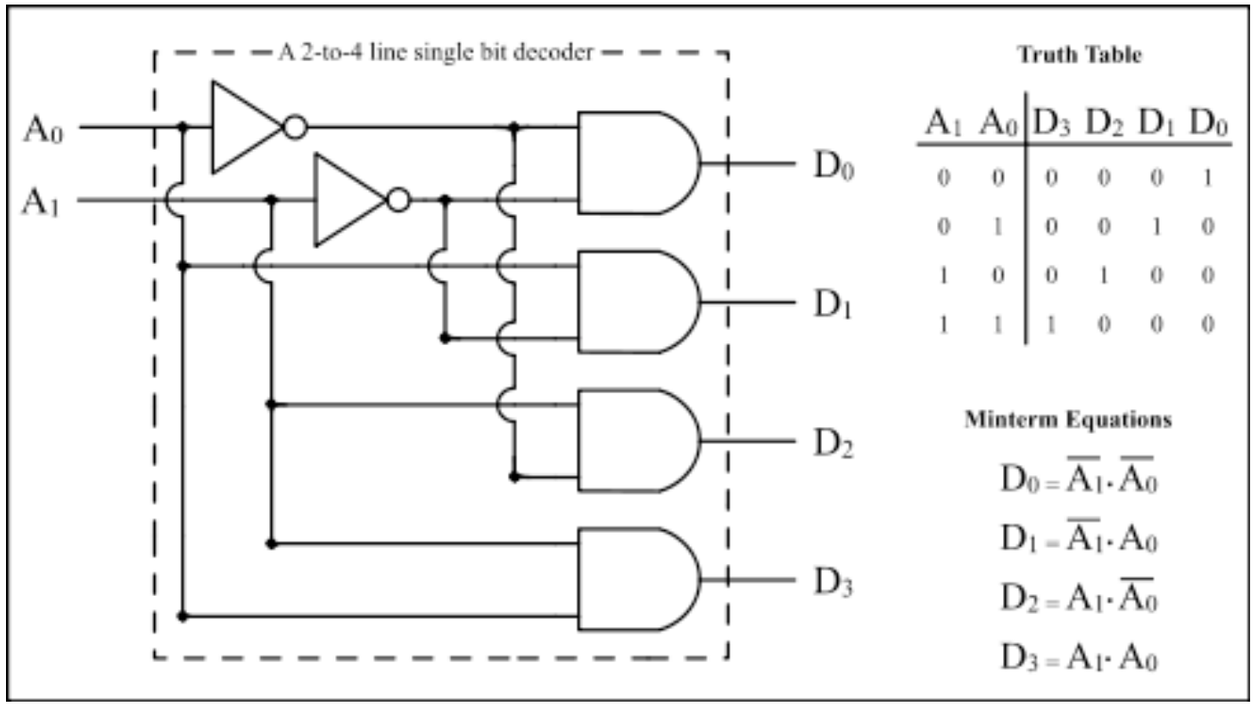
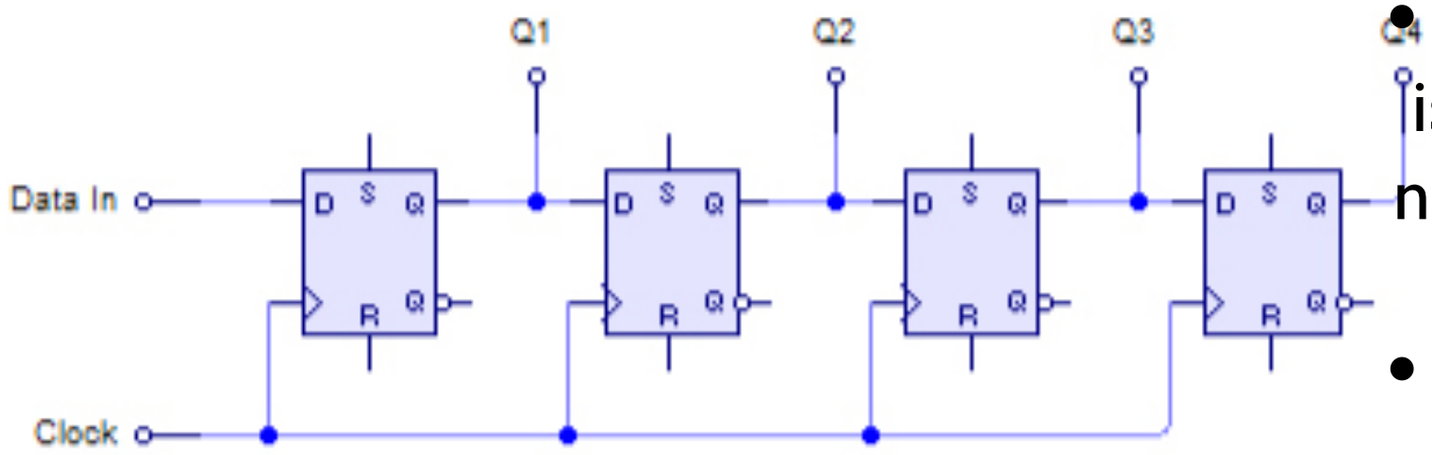


- In a decoder we can only turn ON a single output at the same time

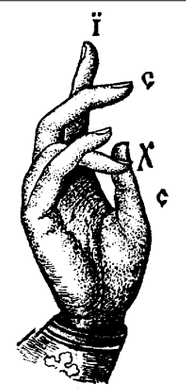
- Turning ON several outputs can be done with time division multiplexing



- In a shift-register, once the value is set, you do not need to feed in new data, so CLK will be kept low

- Shift-register consumes less power (low switching-activity)

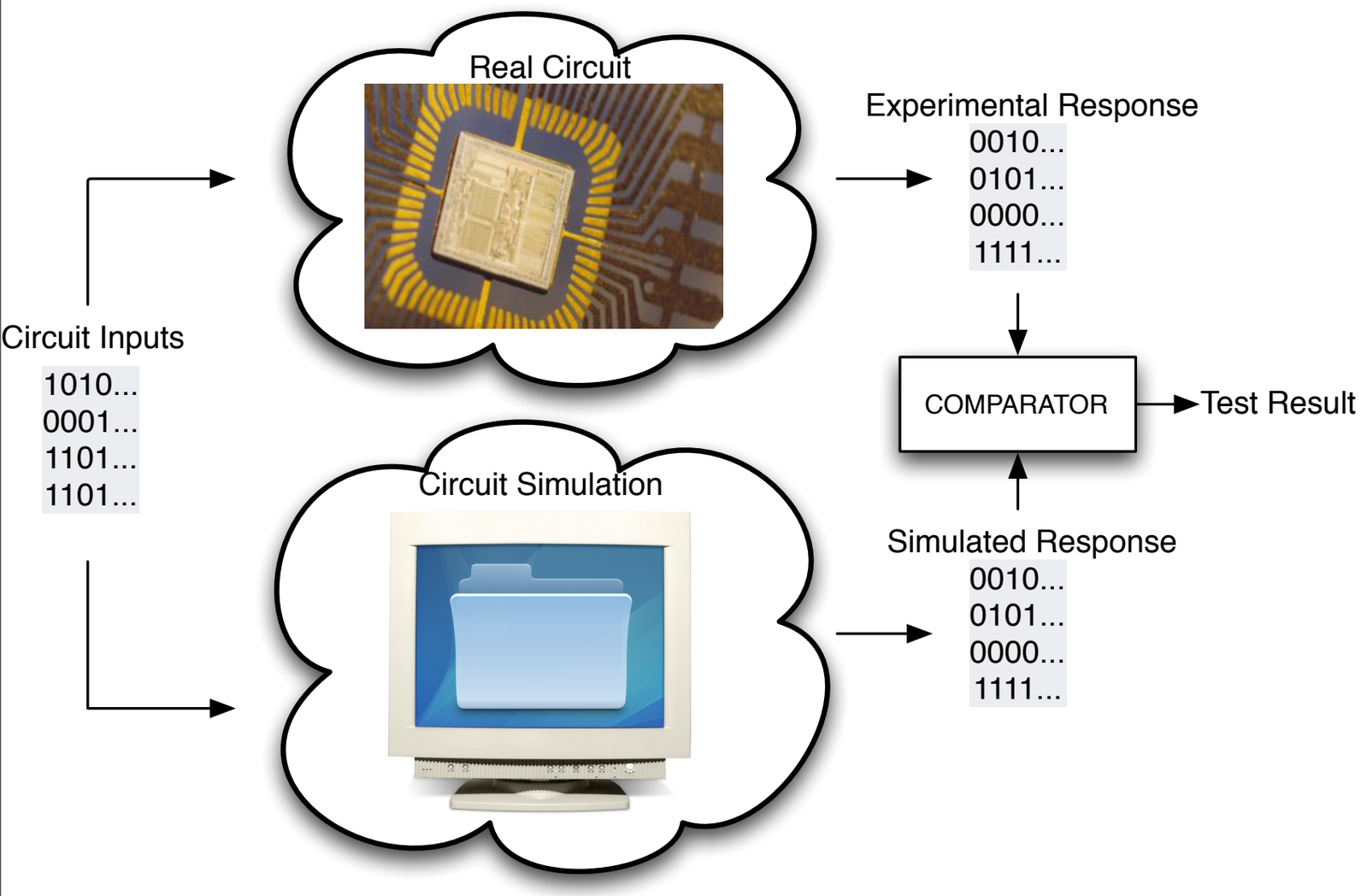
Minor digression: test of electrical circuits



How to test test an electrical circuit?

Minor digression: test of electrical circuits

How to test test an electrical circuit?

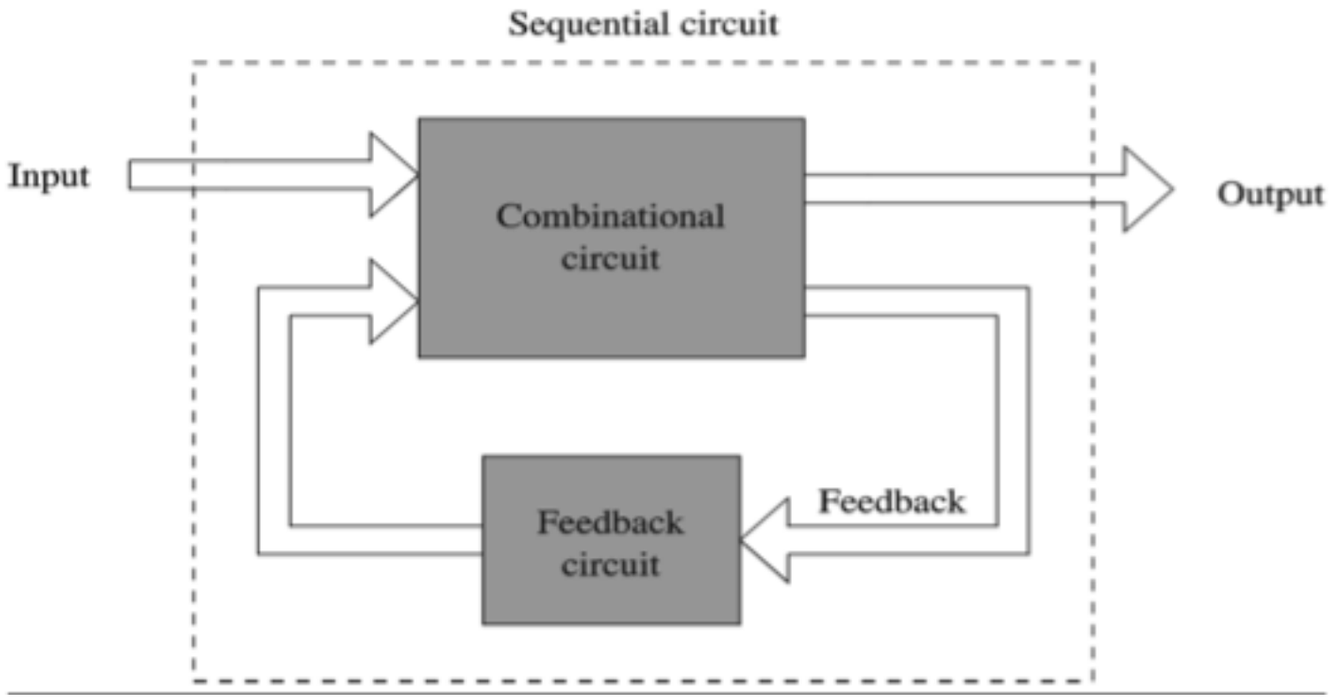


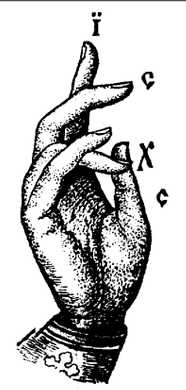
- I get a real circuit and I feed them many test vectors
- A test vector is a bunch of circuit inputs

Testing is "easy" with combinational circuits

- You feed in some test vectors at the input and compare expected with experimental outputs

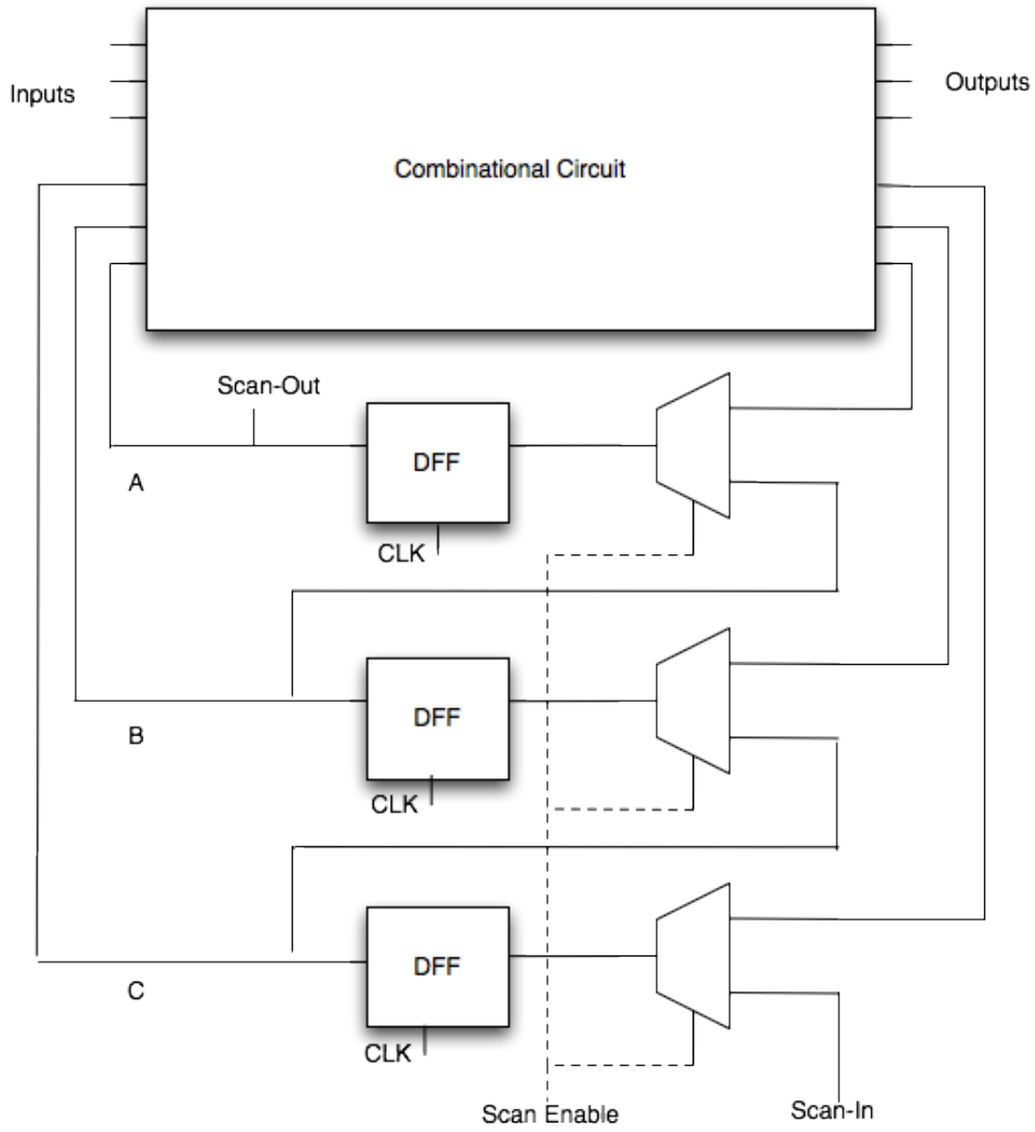
- Not so easy in sequential circuits. Ideally we need to "SET" the values at each Flip-Flop.





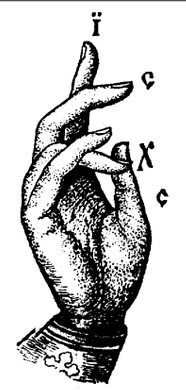
Scan-chains

- The purpose of scan chains is to set a FF value to a given state
- This is used to test the circuit
- For example, how can I set A=0, B=1 and C=1?

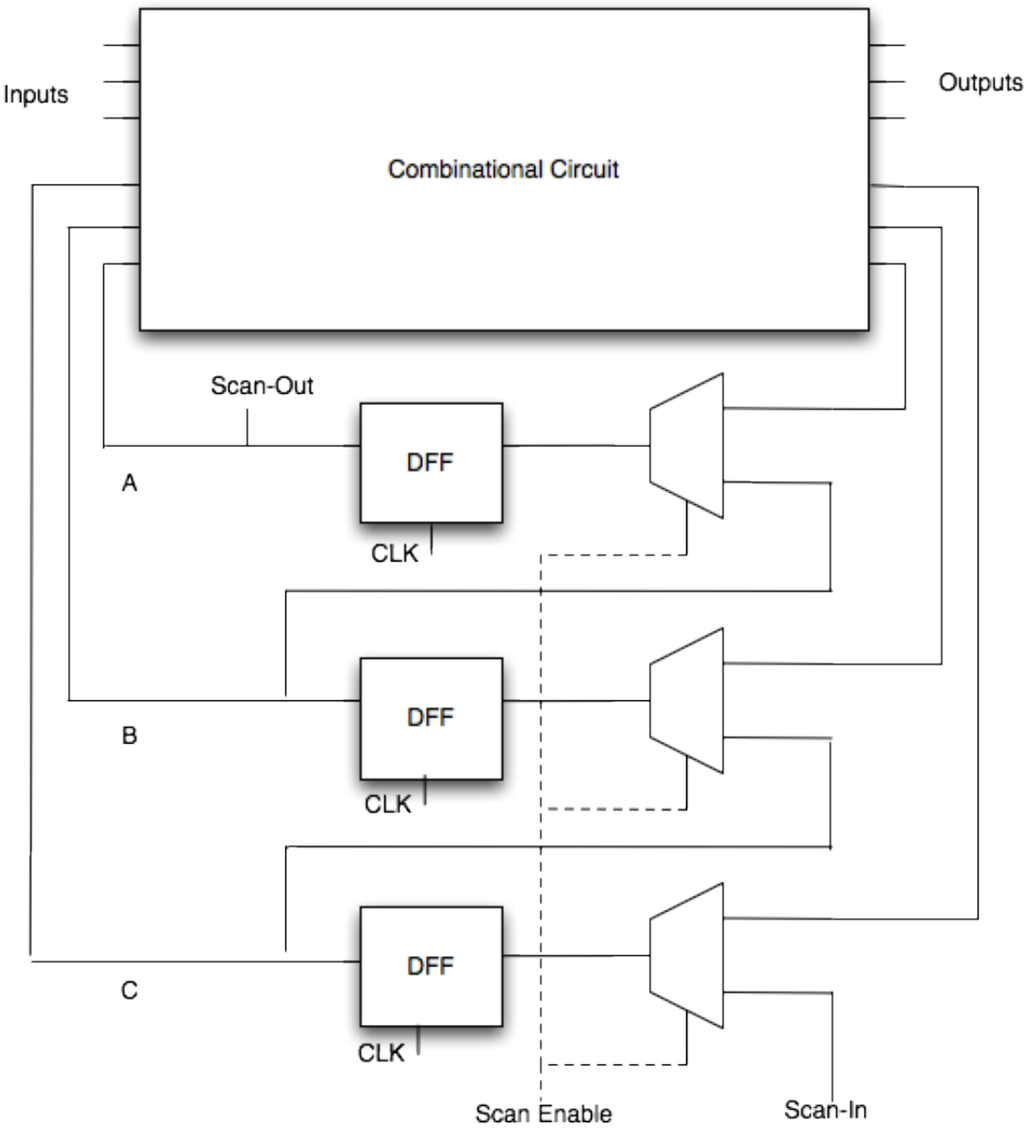


http://lsmwww.epfl.ch/Education/former/2002-2003/VLSIDesign/ch08/ch08.html

Set logic values using a Scan-chain



- How can I set A=0, B=1 and C=1?
- Turn ON Scan Enable
- Send stream 0-1-1, one bit each clock cycle through Scan-In line
- Once done, Turn OFF Scan Enable
- After a while... how do I read logic values at A, B & C?



Read logic values using a Scan-chain

- How can I read values at A, B and C?
  - Turn ON Scan Enable
  - Read value a scan-out each clock cycle
  - Once done, Turn OFF Scan Enable