Practice Exercises

Topic #03 - b) Introduction to Xilinx development environment

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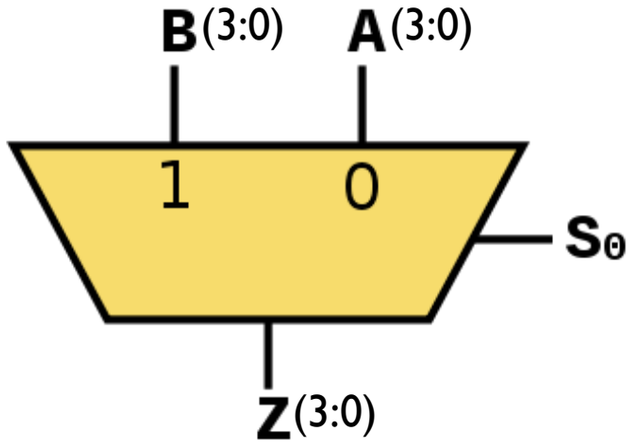
Exercise #1- SPARTAN-3 FPGA implementation of a 2-to-1 MUX



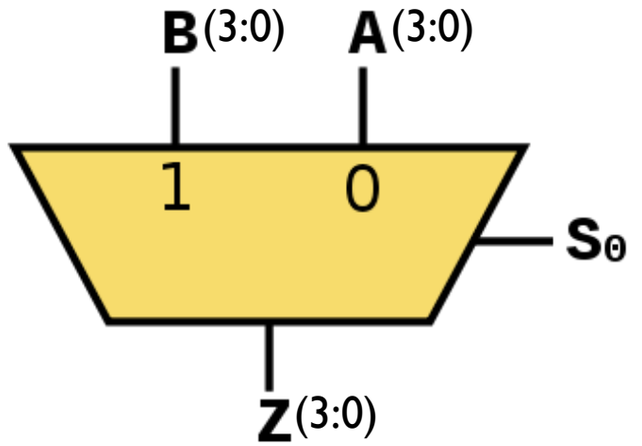
$$Z = (A \cdot \overline{S}) + (B \cdot S)$$

- Inputs **A** and **B** are a 4-bit bus
- Fix the code on the left and map each 4-bit bus to different sets of switches
- Map S0 to button **BTN0**
- Map the output to 4 LEDs

```
library ieee;
use ____________________________;

entity mux is
    port (___, ___: ___ std_logic_vector(3
downto 0);
          sel: in ____________________;
          ___: out std_logic_vector(3 downto
0));
end mux;

architecture example of _____ is
begin
    process (a, b, sel)
    begin
       if (sel='0') then
           c <= a;
       elsif (___________) then
           c <= _____;
       end if;
    end ___________;
end ___________;
```

Solution #1- SPARTAN-3 FPGA implementation of a 2-to-1 MUX

```
library ieee;
use ieee.std_logic_1164.all;

entity mux is
    port (a, b: in std_logic_vector(3 downto 0);
          sel: in bit;
          c: out std_logic_vector(3 downto 0));
end mux;

architecture example of mux is
begin
    process (a, b, sel)
    begin
      if (sel='0') then
          c <= a;
      elsif (sel='1') then
          c <= b;
      end if;
    end process;
end architecture;
```



$$Z = (A \cdot \overline{S}) + (B \cdot S)$$