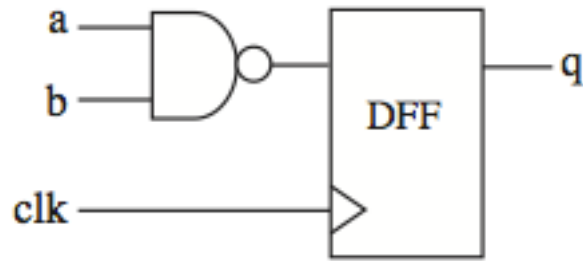


Practice Exercises

Topic #03 - c) Introduction to Aldec Active HDL development environment

Exercise #1 - NAND + DFF

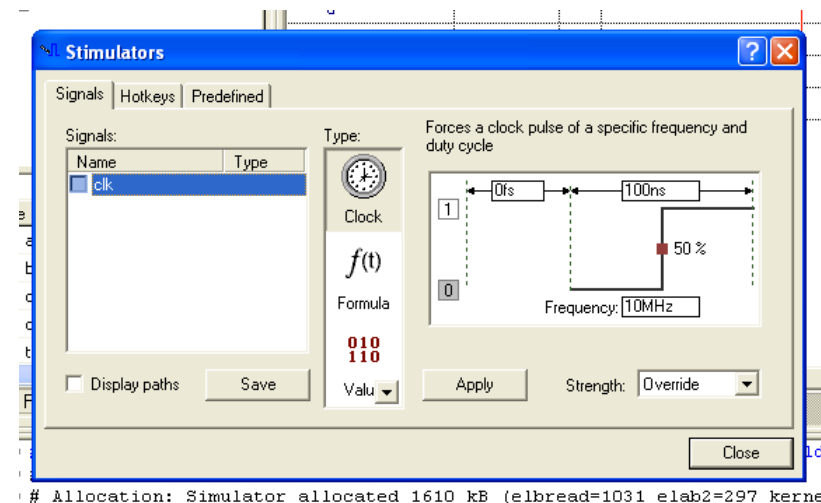


```
entity example is
    port (a,b,clk : in bit;
          q: out bit);
end example;
```

```
architecture example of example is
    signal temp : bit;
```

```
begin
    temp <= a NAND b;
    process (clk)
    begin
        if (clk'event and clk='1') then q<=temp;
        end if;
    end process;
end example;
```

- Re-implement this code but find a way to remove $q \leq temp$
- Display the wave-form. Use the “Clock function” as a stimulus for the clock signal and “hotkey” for the other inputs
- Set the clock period to 20ns



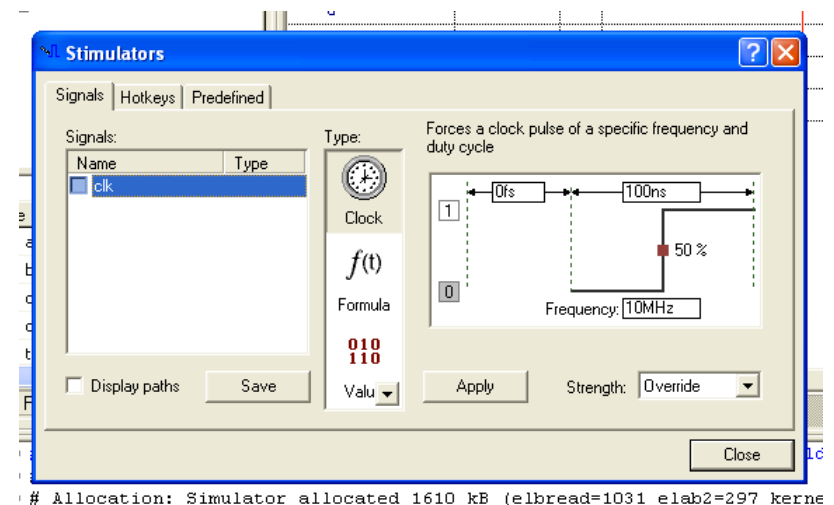
Solution #1 - NAND + DFF (1/3)

```
entity example is
  port (a,b,clk : in bit;
        q: out bit);
end example;
```

architecture example of example is

```
begin
  temp <= a NAND b;
  process (clk)
  begin
    if (clk'event and clk='1') then q<= a NAND b;
    end if;
  end process;
end example;
```

- The code is straight forward



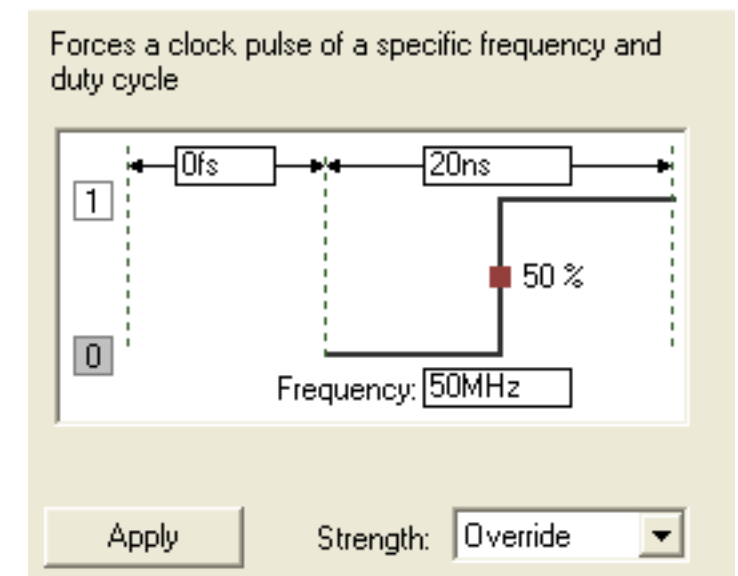
- Setting the stimulus to have a period of 20ns is also easy. You can always try different frequency values and see what is the resulting period (not a very good approach) or ...

Solution #1 - NAND + DFF (2/3)

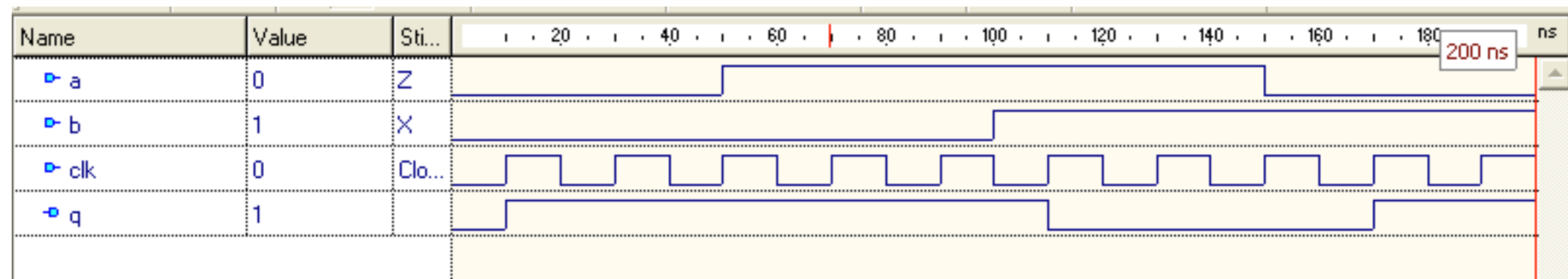
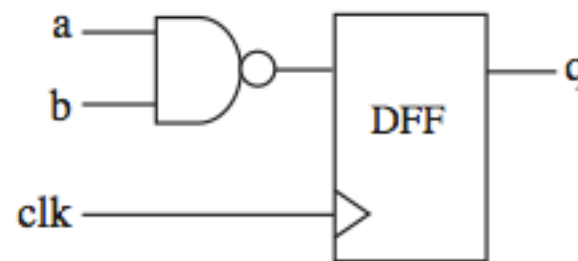
Prefix	Symbol	1000 ^m	10 ⁿ	Decimal
yotta	Y	1000 ⁸	10 ²⁴	1 000 000 000 000 000 000 000 000
zetta	Z	1000 ⁷	10 ²¹	1 000 000 000 000 000 000 000 000
exa	E	1000 ⁶	10 ¹⁸	1 000 000 000 000 000 000 000
peta	P	1000 ⁵	10 ¹⁵	1 000 000 000 000 000 000
tera	T	1000 ⁴	10 ¹²	1 000 000 000 000 000
giga	G	1000 ³	10 ⁹	1 000 000 000
mega	M	1000 ²	10 ⁶	1 000 000
kilo	k	1000 ¹	10 ³	1 000
hecto	h	1000 ^{2/3}	10 ²	100
deca	da	1000 ^{1/3}	10 ¹	10
		1000 ⁰	10 ⁰	1
deci	d	1000 ^{-1/3}	10 ⁻¹	0.1
centi	c	1000 ^{-2/3}	10 ⁻²	0.01
milli	m	1000 ⁻¹	10 ⁻³	0.001
micro	μ	1000 ⁻²	10 ⁻⁶	0.000 001
nano	n	1000 ⁻³	10 ⁻⁹	0.000 000 001
pico	p	1000 ⁻⁴	10 ⁻¹²	0.000 000 000 001
femto	f	1000 ⁻⁵	10 ⁻¹⁵	0.000 000 000 000 001

- Remember that:
- (frequency) = 1 / (period)
- So a period of 20ns is equivalent to

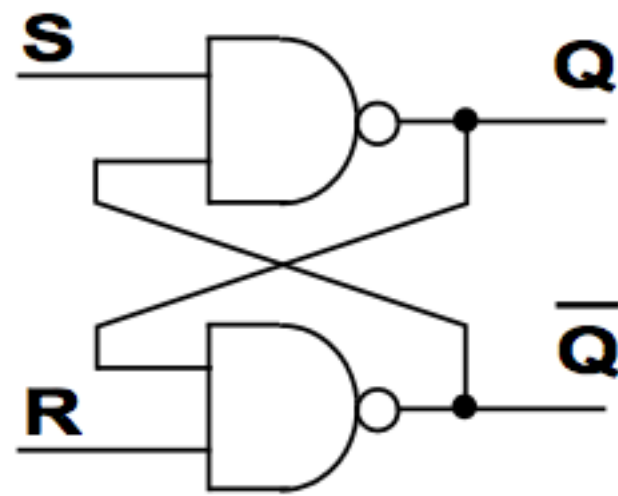
$$\begin{aligned}
 \frac{1}{20 \star 10^{-9}} &= \frac{1}{2 \star 10^{-8}} \\
 &= \frac{1}{2} \star \frac{10^0}{10^{-8}} \\
 &= \frac{1}{2} \star 10^8 \\
 &= 0.5 \star 10^8 \\
 &= 5 \star 10^7 \\
 &= 50 \star 10^6 \\
 &= 50 \text{ MHz}
 \end{aligned}$$



Solution #1 - NAND + DFF (3/3)



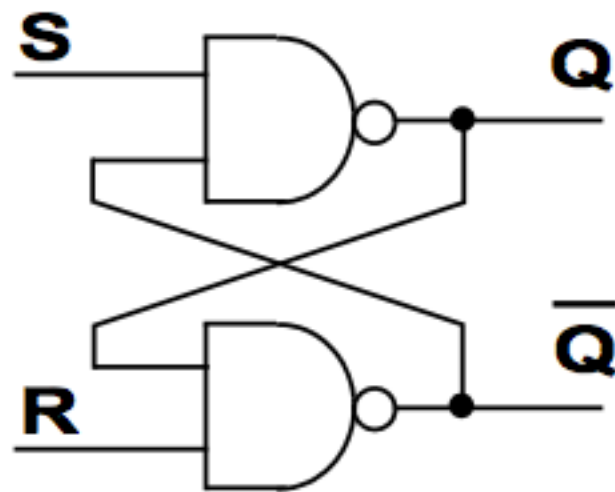
Exercise #2- Set Reset (SR) latch



S	R	Q	$\bar{Q}$	Function
0	0	1-?	1-?	Indeterminate State
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q^+	$\bar{Q}^+$	Storage State

- Implement this SR latch
- Hint: Make sure you appropriately configure the signal modes
- Simulate the circuit and make sure it works as expected

Solution #2- Set Reset (SR) latch



S	R	Q	$\bar{Q}$	Function
0	0	1-?	1-?	Indeterminate State
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q^+	$\bar{Q}^+$	Storage State

entity latch is

```
port (s,r : in bit;
      q,qb : inout bit);
end entity;
```

architecture myarch of latch is
begin

```
q  <= s NAND qb;
qb <= r NAND q;
end architecture;
```

